E U R O P E A N   E D I T I O N

EDN

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

JULY 6, 1995

NEW PRODUCT INTRO

Software-development tool creates C programs automatically pg 15

NEW! COMPONENTS SHOWCASE pg 119

Cover Story:

Delivering the high-speed clock

pg 32

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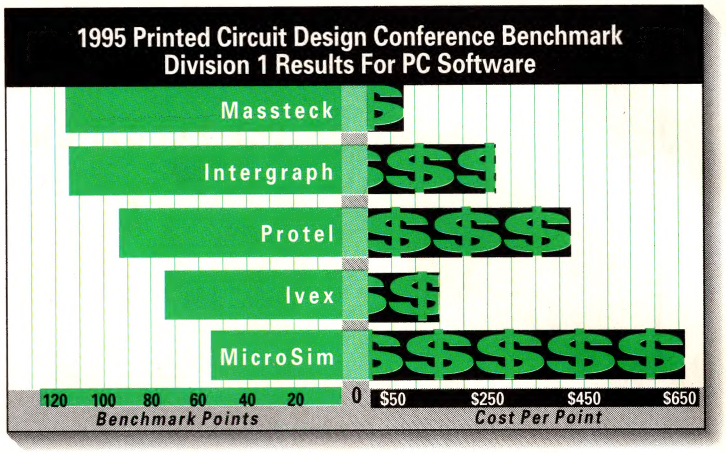

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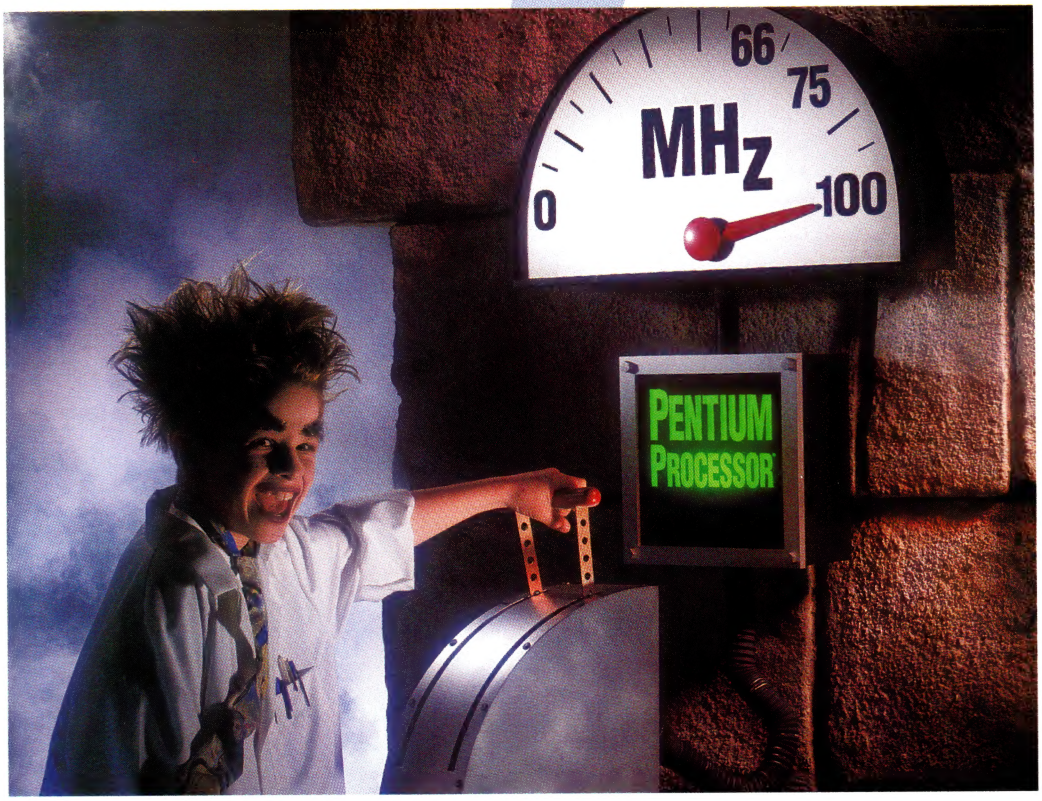

The new Si9145 dc-to-dc switchmode controller IC is the only device that gives you full Pentium® processor performance.

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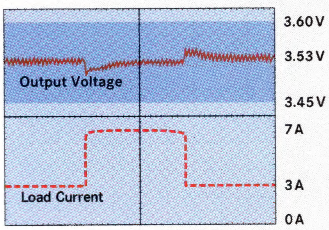

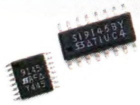

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What's more, the Si9145 is available in both small-outline and TSSOP packages. Combine it with low-profile surface-mount inductors and capacitors, and you have a smaller dc-to-dc converter with the industry's lowest voltage ripple and the best transient response. Just the thing for reducing PCB size!

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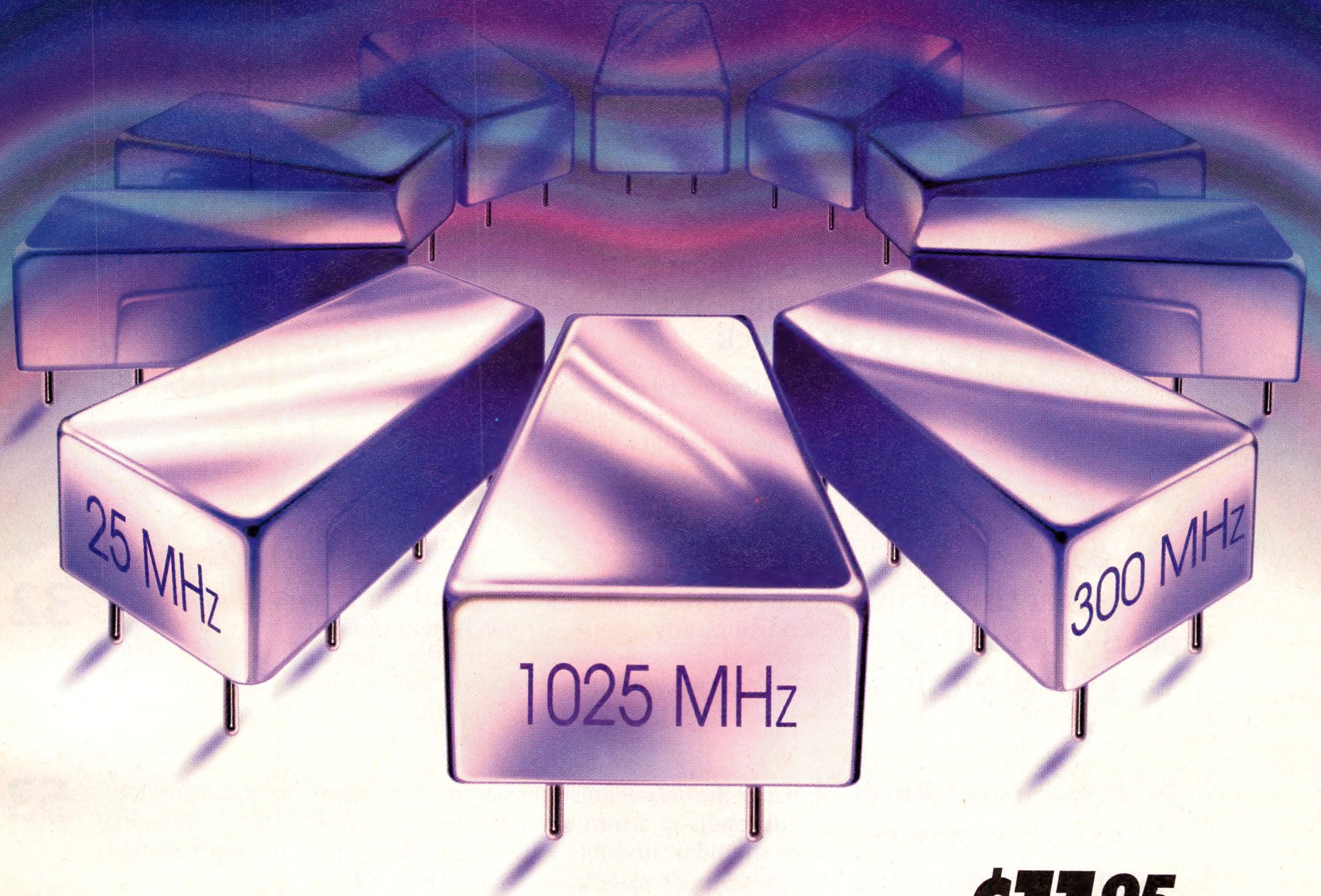

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POS-150	75-150	-103	-23	18	11.95
POS-200	100-200	-102	-24	18	11.95
POS-300	150-280	-100	-30	18	13.95
POS-400	200-380	-98	-28	18	13.95
POS-535	300-525	-93	-26	18	13.95
POS-765	485-765	-85	-21	22	14.95
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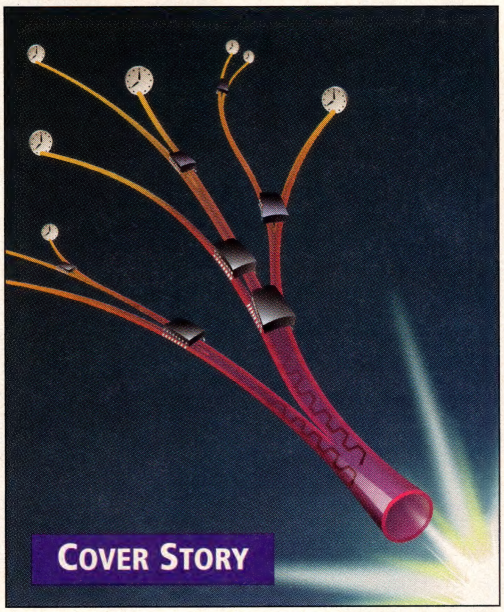
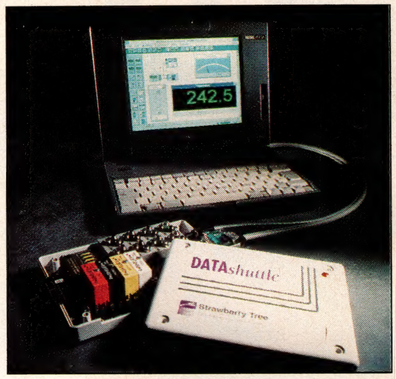


Illustration by Gregg Dinderman
Art direction by Chinsoo Chung
Concept by Bill Schweber



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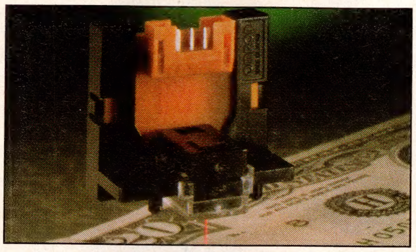

EDN DESIGN IDEAS

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—*Jack Ganssle, Embedded-Systems Contributing Editor*

EDN PRODUCTS

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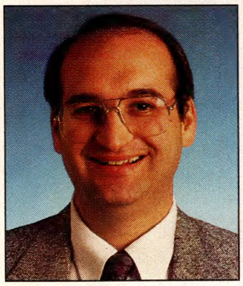
EDN | EDITORIAL

Entertainment, communication, and education: the real convergence



Much has been written about the convergence of computers, communications, and consumer products. This is a supply-side-centric view of the electronics market. In reality, consumers don't care whether you classify a printer/fax/scanner for the home as a computer, communications, or consumer product. They buy it because it performs useful tasks. In fact, the tasks convergence products perform meet the three main consumer needs of modern civilization.

After satisfying the basic needs of food, shelter, transportation, and health, people spend their money on entertainment, communication, and education. I call these three categories the three pillars of modern civilization (the information society). This is a consumption-centric view of the electronics market. Like the converging products that are so hard to classify, it's often very hard to decide which of the three pillars a product represents.

A CD-ROM-based encyclopedia, such as Microsoft's "Encarta," is as entertaining as it is educational. A game such as "Sim City" is as educational as it is entertaining. Interactive TV will satisfy needs in all three categories. A universal TV/video phone/computer clearly falls into all three categories and is likely to become the next big consumer product after the PC. My condolences to the companies scrambling to be king of the set-top-box hill.

After satisfying the basic needs of food, shelter, transportation, and health, people spend their money on entertainment, communication, and education.

Products that fall into one or more of these three categories will be the big sellers of the late 1990s. If you compete in these markets or if your company *should* compete in these markets, take a long look at how well your planned products will satisfy the consumer needs for entertainment, communication, and education.

STEVEN H LEIBSON
EDITOR IN CHIEF

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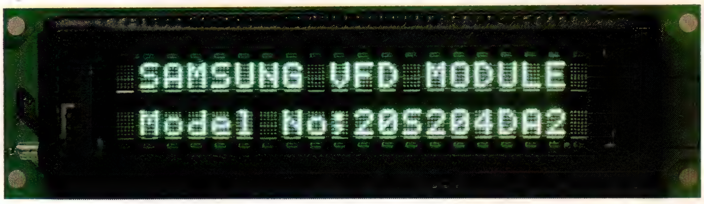

VFD MODULES

MODEL	CHARACTER FORMAT & SYMBOLS	No of Digits (Row X Column)	CHARACTER DIMENSIONS			OUTER DIMENSIONS			ELECTRICAL CHARACTERISTICS			INTERFACE				
			CH (mm)	CW (mm)	CP (mm)	L (mm)	H (mm)	T (mm)	Vcc (Vdc)	Icc (mA)	L (Typ) (ft-L)	Parallel Input	Serial Input	Self Test	Device Select	Busy Out
20S102MA4		1×20	5.0	3.5	4.7	150.0	30.0	26.6	5.0	150	200	○	○	○	○	○
20S204DA2		2×20	5.0	3.5	5.1	155.0	43.0	28.0	5.0	350	250	○	○	○	○	○
40S102MA4		1×40	5.05	3.55	4.75	240.0	40.0	30.0	5.0	350	200	○	○	○	○	○
40S201MA4		2×40	5.05	3.55	4.75	240.0	60.0	29.0	5.0	800	200	○	○	○	○	○
12L101MK1		1×12	11.4	8.7	12.5	200.0	50.0	28.6	5.0	550	250	○	○	○	○	○

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EDN

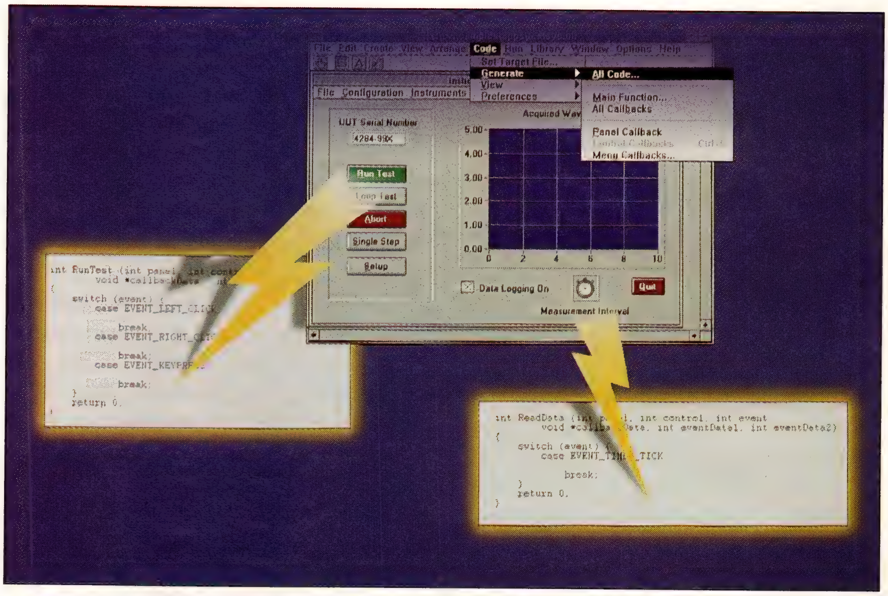
OUT IN FRONT

WHAT'S HOT IN THE DESIGN COMMUNITY

EDITED BY FRAN GRANVILLE

Software-development tool creates C programs automatically

You can write event-driven, graphical-interface ANSI C programs in minutes rather than hours by using CodeBuilder, a utility in Version 3.1 of National Instruments' LabWindows/CVI visual-development software package for Windows PCs and Sun SPARCstations. CodeBuilder not only speeds program writing, but also reduces errors and produces more consistent and maintainable code than human programmers do. You begin by using the User-Interface Editor to assemble knobs, pushbuttons, gauges, and charts on the screen. You then insert acquisition and control code from LabWindows/CVI libraries.



LabWindows/CVI includes customizable ECHO controls that simultaneously provide flexibility and standardization. A CodeBuilder utility pulls in C code that is more consistent and maintainable than code created by human programmers.

New, configurable Extended Control-Hierarchy Objects (ECHOs), including a new timer control, act as instrument drivers, handling low-level hardware programming of data-acquisition boards and making it easy to display acquired data graphically. A new color-intensity plot capability lets you show 3-D plots in 2-D, with color representing the Z-axis position.

Customizable on-screen tool bars present all the common source-code editing and debugging functions. Pointing at a tool-bar button automatically displays tips on how to use the tool. The package provides the tools to develop drivers for VXI instruments in accordance with guidelines of the VXIplug&play Systems Alliance. The package includes the interface-independent I/O drivers of the Virtual Instrument Systems Architecture (VISA) Transition Library (VTL).

To run LabWindows/CVI V3.1, Windows users need 20 Mbytes of hard-disk space and a Borland, Watcom, or Symantec C compiler. Sun users must have 32 Mbytes of disk-swap space and 12 Mbytes of disk space. Sun users who plan to incorporate external C objects must use the Sun ANSI C Compiler or the Gnu C Compiler. Prices begin at $995. Shipments begin this quarter.

—by Dan Strassberg

National Instruments Corp, Austin, TX. (512) 794-0100. **Circle No. 445**

BBS is back on-line

EDN's computer bulletin-board system (BBS) is now back on-line, after having experienced some technical difficulties. We apologize for any inconvenience you may have experienced. To access the BBS, phone (617) 558-4241 with modem settings 300/1200/2400 8,N,1, (9600 baud=(617) 558-4580).

Analog-line-card telecomm codec simplifies design

AT&T Microelectronics' T7504 codec performs A/D conversion for four voice channels (μ-law/A-law companding PCM), using a single 5V supply. The device suits analog line cards for use in central-office, loop-carrier, and private-phone-exchange applications. In addition to the converters, the IC includes transmit and

(continued on pg 16)

receive filters, S/H and autozero circuitry, and a precision reference to interface voice-telephone circuits to a time-division-multiplexed system. The T7504 assigns PCM data to any time slot on a per-channel basis, operating from a 2.048- or 4.096-MHz master clock.

The device, which comes in a 28-pin DIP or PLCC, requires 37-mW/channel typical operating power; you can power down each channel to cut power consumption to 1 mW/channel. The codec has differential architecture for high noise immunity and meets D3/D4 and CCITT G.711-G.714 requirements. AT&T fabricates the T7504 in latch-up-free CMOS technology; it costs $6.20 (10,000).

—by Bill Schweber

AT&T Microelectronics, Allentown, PA. (800) 372-2447.

Circle No. 446

Cyrix offers 586-class processor

When it arrives in the third quarter, the M1 processor from Cyrix will potentially outperform Intel's Pentium at the expense of a considerably larger die size. This strategy has taken Cyrix beyond the reach of 586-class pricing. To compete effectively at the 586 level, Cyrix followed the successful approach it took with its 486 and made it pin-compatible with the 386. Specifically, Cyrix has developed the 5x86, a scaled-down M1 with a 64-bit internal architecture in a 486 footprint. Although the 5x86 has only a 32-bit external bus, the CPU features static-branch prediction, an 80-bit floating-point unit, and a 16-kbyte, unified, write-back cache. Cyrix expects the 100-MHz 5x86 to deliver performance comparable to a 75-MHz Pentium and sell for $147 (1000).

—by Markus Levy

Cyrix Corp, Richardson, TX. (800) 462-9749.

Circle No. 447

Delay calculator targets submicron designs

Integrated Silicon Systems (ISS) has developed ΨTime, a delay calculator that addresses the problems of calculating delays in interconnect-dominated submicron chips. These problems are due to the difficulty in simultaneously and accurately modeling the gate delay, interconnect delay, and input waveform on a net. The ΨTime product lets you more accurately calculate on-chip delays by combining the gate-timing model, the RC network being driven, and the input rise time to generate a driving-point waveform for each extracted net. Separately calculating resistance and capacitance, ΨTime interactively tunes the driver model while determining the RC network's "effective" capacitance. The tool then uses the converged effective capacitance and gate-timing model, using the updated driver model to drive the RC network to calculate gate delay and interconnect delay. The ΨTime product calculates point-to-point interconnect delays from the driving point in the circuit to each load point in the RC network. It also calculates separate values for effective capacitance, gate delays, and interconnect delays for each specified input edge rate on a net.

Input RC data formats to ΨTime include Spice and Standard Parasitic Format (SPF). You can input k-factor, table, Thevenin, and ISS's ΨDrive models to ΨTime. You can output Standard Delay Format (SDF) and Motive IDD and ISS formats. The tool can be used with both prelayout RC estimates and postlayout RC-extracted data. The ΨTime product runs on Digital Equipment Corp, Hewlett-Packard, IBM, and Sun workstations. Prices start at $25,000.

—by Jim Lipman

Integrated Silicon Systems, Research Triangle Park, NC. (919) 941-6600.

Circle No. 448

DILBERT® by Scott Adams

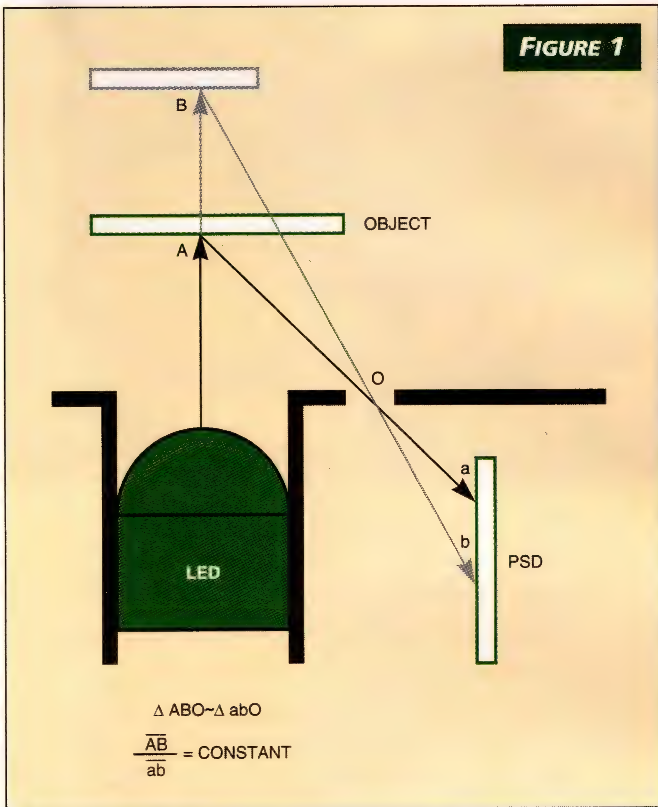
EMAIL: scottadams@aol.com

Optical sensor detects 10-μm displacement

A new optical sensor combines an LED with a position-sensing diode (PSD) to detect position changes as small as 10 μm. Unlike other optical sensors that work by measuring the intensity of reflected light, the Z4D-A01 from Omron Electronics measures the position of a reflected spot of light on the surface of the device's PSD chip. The Z4D-A01 then uses the geometric principle of similar triangles to determine displacement of a sensed object from an initial location (**Fig 1**). Omron anticipates use of the sensor in products that measure the thickness or position of a sheet of paper. Omron marketer Chris Corder expects to see the device in copiers, printers, fax machines, and money changers.

Omron's Z4D-A01 optical sensor targets applications that need to measure the thickness of paper.

Unlike sensors that provide a single output from a photodiode or phototransistor, the Z4D-A01 provides two outputs from its PSD. Each output current is inversely proportional to the distance from the current's corresponding electrode to an incident spot of light on the PSD's surface. The Z4D-A01's LED creates the spot by reflecting light off the object whose displacement must be measured. As the object moves, so does the incident spot of light, thus altering the PSD's two output currents. The ratio of the two currents determines the spot's location, and application of the principle of similar triangles (ABO and abO in **Fig 1**) then allows computation of the sensed object's displacement (AB) from a previous location.



By applying the two outputs of a position-sensing diode to the principle of similar triangles, the Z4D-A01 optical sensor can measure very small object displacements.

The $45 Z4D-A01 has a maximum sensing distance of about 6.5 mm. It works with a microcontroller that needs an A/D converter having at least 10 bits to take advantage of the sensor's maximum resolution. The screw-mount sensor operates on 5V dc and has an attached standard connector for use in remote-sensing applications.
—by Gary Legg

Omron Electronics Inc, Schaumburg, IL. (800) 556-6766. **Circle No. 449**

PC chip set includes complete secondary cache

Cypress Semiconductor has introduced a Pentium-based PC chip set that integrates all standard I/O and bus interfaces along with a complete 128-kbyte secondary-cache-memory subsystem. Cypress expects the three-chip 3.3V hyperCache chip set to cost $48 (1000) and be available for initial sampling in August.

The set's first chip, the CY82C691, performs system and memory-interface functions. It provides CPU and PCI bus interfaces, a cache controller that can handle as much as 1 Mbyte of secondary cache, and an integral 8k×21-bit cache tag RAM. The device also provides DRAM control for as many as six banks (768 Mbytes max) of mixed fast-page and extended-data-out DRAMs. The controller also allows direct DRAM access for unified graphics/main-memory designs.

The CY82C692 provides a 128-kbyte, two-way set-associative, pipelined cache memory with 3-1-1-1 performance at 66-MHz bus-clock speeds. In addition to the memory block, the device offers a wraparound counter for both Intel and linear burst access, eight-deep FIFO memories for PCI bus

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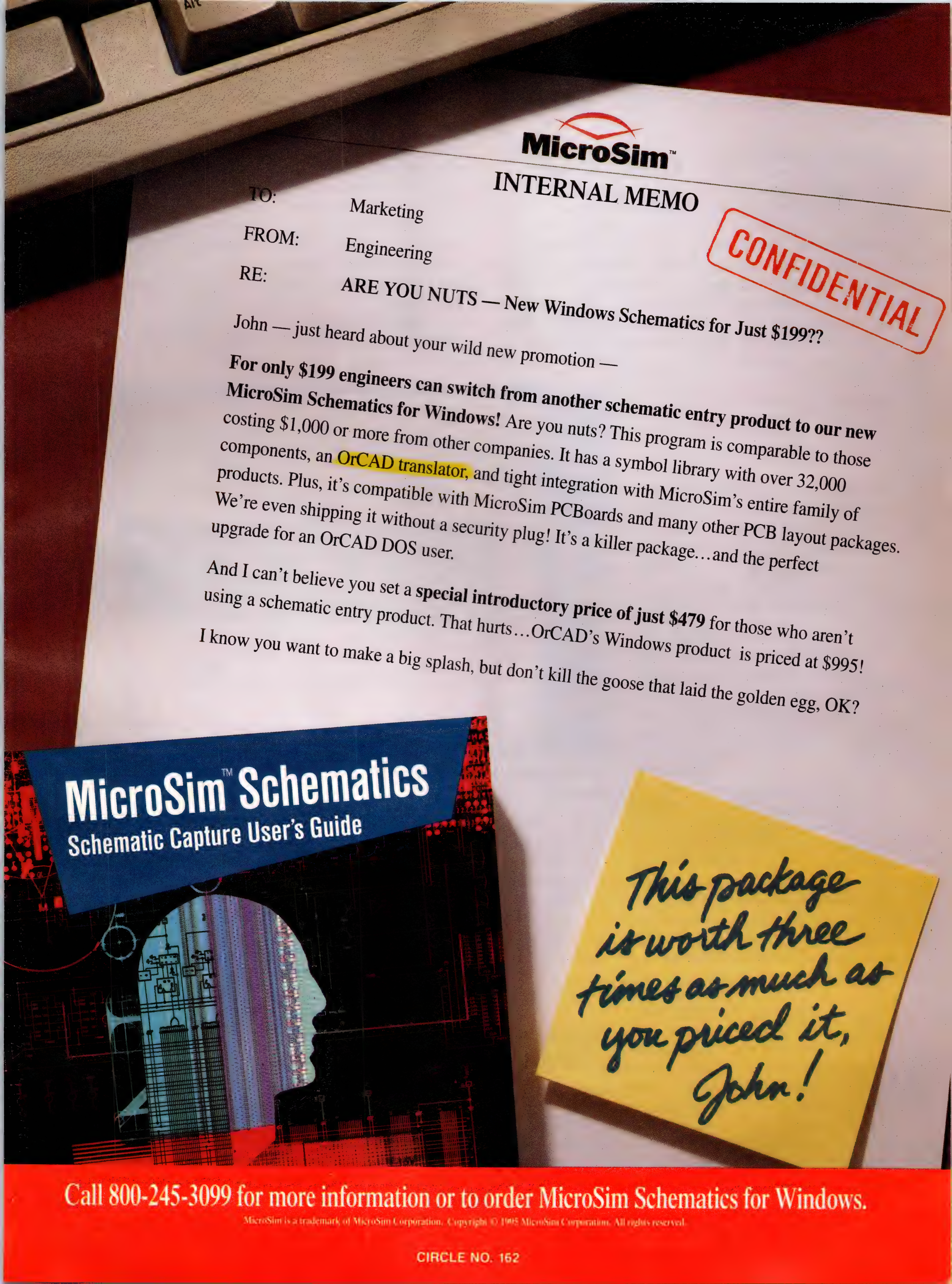

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CIRCLE NO. 162

buffering, parity checking, bus-size conversion logic, and data-steering logic. The C692 also offers a 64-bit port to an optional, $14 CY82C694 128-kbyte expansion cache memory. The C694 performs as the C692 but has only the memory block.

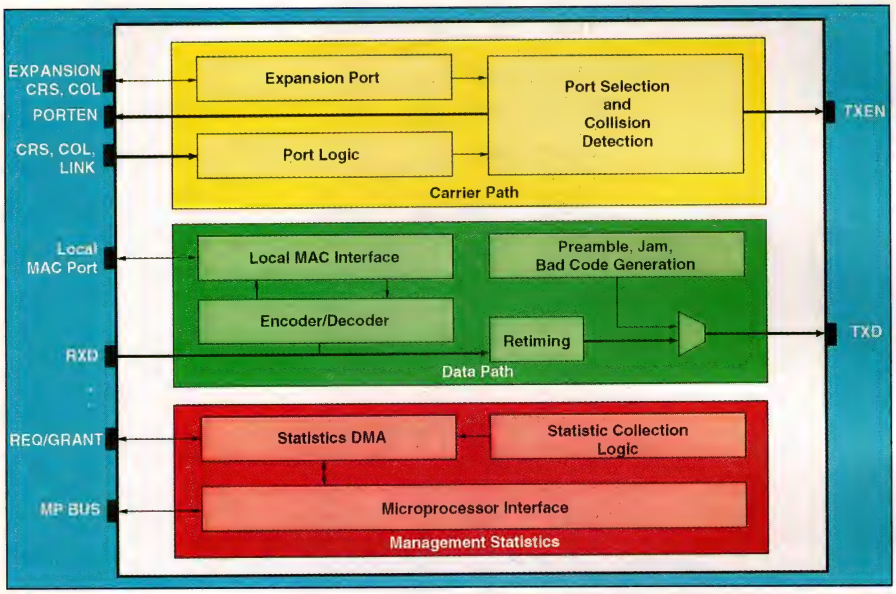
The third chip, the CY8C693, integrates I/O bus and peripheral control. It offers both ISA and PCI bus interfaces, handling as many as five PCI bus masters. It also includes DMA and interrupt control along with a tunable real-time clock, battery-backed SRAM, PS/2 mouse and keyboard interfaces, an IDE interface with bus mastering, and power-management circuitry. The chip's on-board bus drivers offer selectable 8-, 12-, and 24-mA drive levels, eliminating the need for external bus drivers.

Cypress's schedule for the hyperCache chip set calls for production ramp-up beginning in November. Cypress also plans to migrate the design to its RAM3 process in 1996 to produce a single-chip version.

—by Richard A Quinnell

Cypress Semiconductor, San Jose, CA. (408) 943-2600. **Circle No. 450**

Repeater controller handles fast Ethernet connections



The BCM5012 100BaseT repeater controller has its own system-management resources.

The one-chip BCM5012 repeater controller from Broadcom supports 100BaseT4, 100BaseTX, and 100-Base-FX fast Ethernet connections and network management. With the company's BCM5000 10/100BaseT4 fast-Φ transceiver chip, the repeater controller enables network manufacturers to design 100-Mbps networks.

The BCM5012 meets IEEE 802.3 specifications and connects to any media type, including CAT 3, 4, and 5 unshielded twisted pair (UTP), shielded twisted pair, and fiber-optic media.

The device integrates features that allow system managers to operate and troubleshoot networks using the same software across multiple physical layers. The BCM5012 facilitates network management by Simple Network Management Protocol software through a collection of all the IEEE 802.3 management-information blocks. The chip also includes dedicated port connections for a local media-access-control layer and μP.

The chip can handle 10 stackable repeater hubs with 13 repeater ports on each hub and thus handles the popular repeater model that uses 12 ports of a primary fast-Ethernet connection. You can use the other port as a translational port that handles other connections or a fiber-optic uplink. Using this repeater model in a 10-stacked hub configuration, manufacturers can support 130 ports with various fast-Ethernet connections in a single stack.

A typical 12-port 100BaseT4 repeater-hub application uses a BCM5012 and 12 of the company's BCM5000 chips. The single-chip BCM5000 handles 100BaseT4, 10BaseT, and 10BaseT full-duplex Ethernet on CAT 3, 4, and 5 UTP cable. The company uses DSP for adaptive equalization. DSP enables 100BaseT4 connections to achieve an S/N ratio that's 3 dB better than that of the ideal linear analog method. The BCM5012 comes in a 208-pin PQFP and costs $108 (1000).

—by John Gallant

Broadcom Corp, Los Angeles CA. (310) 443-4490.

Circle No. 451

Spread-spectrum IC is core of transparent-modem link

Using techniques of narrowband FM along with analog circuitry, Wireless Logic's WLT9009 can serve as the core of a full-duplex wireless link. A complete system using this IC functions as a 900-MHz spread-spectrum wireless link, interfacing between a roving unit (such as a PC) and a wired modem. It is transparent to both link endpoints and supports modem modulation and protocols up to 19.2 kbps. Application range is several hundred meters, even within buildings.

(continued on pg 22)

12 Bits, 1 µA, 3 V – 5 V

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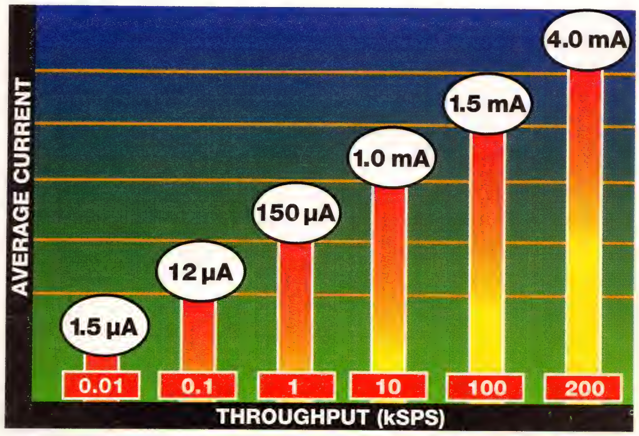
Introducing the AD785x, the first family of 12-bit ADCs to combine the high performance, minimal power consumption, small package size and low cost required for today's portable applications.

More Samples per µA

As the chart shows, the AD785x series delivers excellent throughput with negligible current consumption – up to twice the samples per µA as the competition. In addition, the partial- and full-sleep modes enable you to bring power consumption to an absolute minimum. Whether your system calls for 3-V or 5-V operation, all members of the AD785x family offer the industry's best throughput-to-current ratio.



	AD7853/L	AD7858/L	AD7854/L	AD7859/L	AD7896
Throughput (kSPS)	200/100	200/100	200/100	200/100	100
Power @ 3 V (mW max)	16.5/5.4	16.5/5.4	16.5/5.4	6.5/5.4	12
Supply Range (Volts)	(All are 3.3 V ± 10% & 5 V ± 10%)				2.7-5.5
Channels-Interface	1-Serial	8-Serial	1-Parallel	8-Parallel	1-Serial
Smallest Package	24-SSOP	24-SSOP	28-SSOP	44-PQFP	8-SOIC
Price* ($)	8.95/6.45	9.85/6.95	9.35/7.45	11.60/8.75	6.75

System Calibration

Self- and system-calibration features, including autocalibration on power-up, ensure accurate operation over temperature and time. Add in superior ac/dc characteristics like 70 dB SNR and ±0.5 LSB INL, and you also have an ideal ADC for instrumentation applications.

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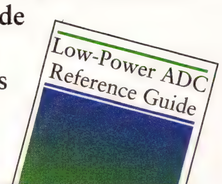

For a Low-Power ADC Reference Guide with sample and technical information, contact the Analog Devices office or sales representative listed below.

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CIRCLE NO. 205

Using this chip, user data modulates a high frequency via a VCO, and the VCO output mixes with a pseudorandom-noise (PN) sequence. The result is a biphase FM signal. The corresponding receiver down-converts the FM signal and then demodulates it back to baseband. Unlike baseband despread techniques, which result in relatively wide, 4-MHz signals that are open to noise and hard to filter, this RF despread provides superior noise and range performance, with 30-kHz IF reducing interference energy. Process gain is 23 dB.

The WLT9009 spread-spectrum signal processor contains two PN sequence generators, with 2048- and 8192-bit sequence lengths, and has a patent-pending frequency-diversity scheme for increased robustness. The device comes in a 64-lead PQFP and costs $16 (10,000).

—by Bill Schweber

Wireless Logic Inc, San Jose, CA. (408) 246-1538. **Circle No. 452**

Visual-media accelerator employs 170-MHz RAMDAC

Cirrus Logic bases its new CL-GD5462 64-bit visual-media accelerator on a 500-Mbyte/sec memory architecture. The device lets a PC simultaneously display three video windows at 30 frames/sec with high-resolution graphics. The 64-bit graphics engine includes a 170-MHz RAMDAC and offers a 500-Mbyte/sec memory bandwidth. The chip also has dual 170- and 250-MHz programmable clock synthesizers to support noninterlaced graphics resolution as high as 1600×1200 pixels. It also handles color depths as high as 32 bits/pixel, which includes 24-bit true color with an 8-bit alpha channel. The chip supports vertical refresh rates greater than 85 Hz.

Standard features include support for Peripheral Component Interconnect (PCI) 2.1 and VL bus interfaces with optimization for PCI burst modes, plug-and-play compatibility, "green-PC" power-management functions, and support for a multimedia interface.

You can scale all display windows in X and Y directions from icon size to full screen, and you can arbitrarily occlude—position and overlap—video windows anywhere on the screen. The chip also converts YUV-encoded data to RGB data for PCs. The CL-GD5462 costs $49 (1000).—by John Gallant

Cirrus Logic Inc, Fremont, CA. (510) 226-2123. Circle No. 453

50M-sample/sec arbitrary-waveform generator doubles as 64-bit pattern generator

Deep within most arbitrary-waveform generators lies the heart of a digital pattern generator. Only a few vendors provide hardware that lets you unlock the pattern-generation capabilities, however. Also, most waveform generators that produce digital patterns create rather narrow ones. In the case of Wavetek Corp's Model 296, though, the patterns can be 64 bits

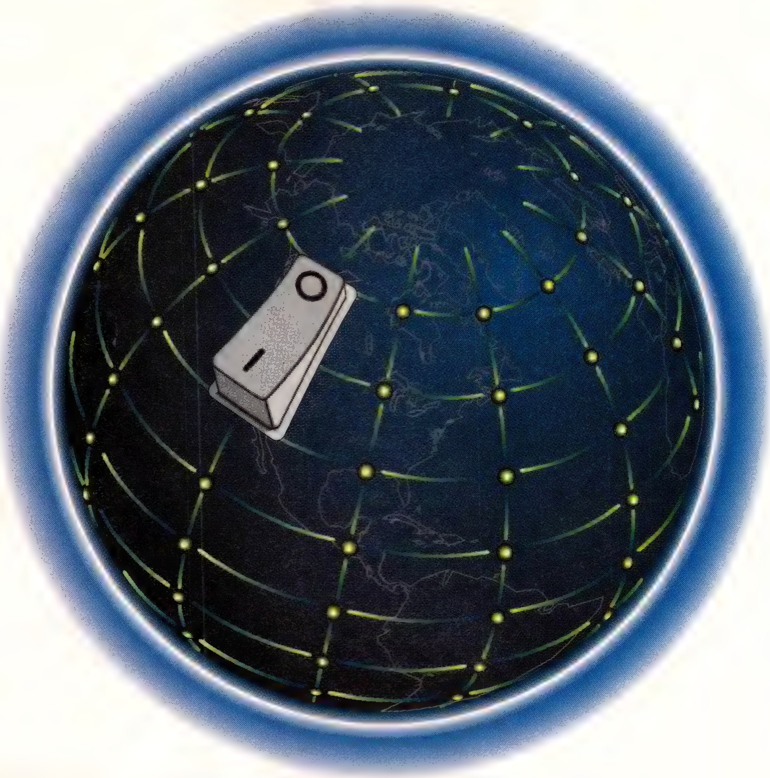
A graphics screen and graphical user interface simplify waveform creation and editing with Wavetek's Model 296 four-channel, 50M-sample/sec arbitrary-waveform generator. The generator can also function as a generator of 64-bit-wide digital patterns or of waveforms and patterns simultaneously.

wide. That's because the 50M-sample/sec generator has four independent channels, and you can phase-lock their variable-frequency clocks. Each channel can generate 12-bit-resolution analog waveforms or 16-bit-wide digital patterns, so you can simultaneously create analog waveforms and digital patterns. Maximum waveform amplitude is 15V p-p (80V p-p optional).

Each channel has a 128k-word-deep pattern memory; a 512k-word-deep memory is optional. To effectively increase the pattern depth still further, you can divide the memory into waveform segments and link up to 4095 segments into one waveform. You can also create complicated waveforms by summing the outputs of two or more channels on the internal bus. The generator can download waveforms via its floppy-disk drive or RS-232C and IEEE-488 interfaces. A built-in graphics screen and mouse-controlled graphical user interface simplify waveform creation and editing. $7245.

—by Dan Strassberg

Wavetek Corp, San Diego, CA. (619) 279-2200. Circle No. 454



Five vendors announce PCMCIA data-acquisition cards

If you judge by the number of companies introducing PCMCIA data-acquisition cards, the tiny plug-ins constitute one *hot* product category. In a recent four-week period, at least five companies announced such cards.

For example, both Intelligent Instrumentation and Soltec announced pairs of 12-bit models for $595 each. Each unit scans eight differential inputs and takes 30k samples/sec. Each company offers one card that provides gains of 1, 2, 4, and 8 and another that provides gains of 1, 10, 100, and 1000. All of these cards provide four digital inputs and four digital outputs. The vendors also supply signal-termination units. For $225, you can buy extra copies of Intelligent Instrumentation's unit, which includes thermocouple cold-junction compensation and a voltage reference.

IOtech has announced two cards—a 12-bit unit that costs $695 and a 16-bit unit that costs $895. Each card takes 100k samples/sec and accepts eight differential or 16 single-ended inputs.

Keithley Metrabyte has announced three 12-bit cards, each at $599. All accept eight differential or 16 single-ended analog signals and provide eight digital outputs and four digital inputs. Two units take 34k samples/sec and offer programmable gain (1, 2, 4, and 8 on one; 1, 10, 100, and 1000 on the other). The third unit offers a fixed gain of 1 but takes 140k samples/sec.

National Instruments has expanded its line to five cards, three of which convert analog inputs with 12-bit resolution. Of these, two take 100k samples/sec: A $695 unit that accepts eight single-ended or four differential analog inputs also offers two DAC outputs, 24 digital I/O lines, and three counter/timers. A $595 unit that accepts 16 single-ended or eight differential inputs offers 16 digital I/O lines and two counter/timers. A $395 50k-sample/sec unit that accepts eight single-ended inputs offers eight digital I/O lines and two counter/timers. Models without ADCs include a $195 unit that provides 24 digital I/O lines and a $325 unit that provides 16 digital I/O lines and two DAC outputs. For more information on these products, also see "Portable hardware makes experiments interactive," pg 53.—by Dan Strassberg

Intelligent Instrumentation, Tucson, AZ. (520) 573-0887. **Circle No. 455**

IOtech Inc, Cleveland, OH. (216) 439-4091. **Circle No. 456**

Keithley Metrabyte, Taunton, MA. (508) 880-3000. **Circle No. 457**

National Instruments Corp, Austin, TX. (512) 794-0100. **Circle No. 458**

Soltec Corp, San Fernando, CA. (818) 365-0800. **Circle No. 459**

Flash devices target serial EEPROM

Xicor has announced samples of SerialFlash, the first commercially available serial flash memory. These devices use the serial-peripheral-interface (SPI) bus protocol or the two-wire serial interface to allow access to and writing of the memory's stored data. The devices operate at a maximum data rate of only 1 MHz, but this speed is sufficient for the EEPROM applications SerialFlash targets. Other features include a 1.8 to 3.6V program and read operation, data protection on each of four write blocks, and 0.9-mm TSSOP packaging. The serial flash is available in 8-, 16-, 32-, and 64-kbyte densities for $2.95, $2.50, $1.75, and $1.50, respectively. Xicor designates the devices as X2yF008, X2yF016, X2yF032, and X2yF064 (where y=5 for the SPI version and y=4 for the two-wire version).—by Markus Levy

Xicor Inc, Milpitas, CA. (408) 432-8888. **Circle No. 462**

Math software integrates with Lotus Notes and the World Wide Web

With its latest release, a mathematical software package that has won the hearts of engineers and experimenters turns into something unusual, if not unique—groupware for techies. MathCad V6.0 integrates with Lotus Notes to allow workgroup members to review, revise, and comment on MathCad documents and to distribute modified and annotated documents among their peers. Without leaving MathCad, you can also download and manipulate work sheets from the Internet's World Wide Web. You can merge such work sheets or portions of them into your own documents and you can follow hot links to other MathCad documents. A further benefit of compatibility with Notes is MathCad's ability to track a document's revision history.

The new release also adds advanced visualization and animation tools and an interactive programming language based on extensible math notation. MathCad V6.0 is a 32-bit Windows application that runs under Windows V3.1, Windows for Workgroups, Windows NT, and Windows 95. A Macintosh version of the products will appear in early 1996. MathCad V6.0 Plus Professional Edition costs $349.95; registered users of V5.0 who wish to upgrade pay $149.95. MathCad V6.0 Standard Edition costs $129.95 and $49.95 to V5.0 users who wish to upgrade.—by Dan Strassberg

Mathsoft Inc, Cambridge, MA. (617) 577-1017. **Circle No. 460**

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FPGA co-processor targets embedded control

Xilinx's SRAM-based XC6200 family of field-programmable gate arrays (FPGAs) for co-processing applications is the first µP-compatible FPGA series for the embedded-control market. The targeted applications include high-bandwidth and computation-intensive functions, such as laser printers, video- and image-processing systems, telecommunications equipment, and encryption/decryption and encoding/decoding circuits.

Unlike conventional FPGA architectures, the XC6200 family has a standard µP interface, which simplifies overall hardware design. The XC6200 also includes the FastMap memory-mapped I/O interface. FastMap comprises a µP-compatible address bus, a data bus, and control lines. Direct access to all internal logic registers through the FastMap bus interface permits simple access by C-language application programs.

The architecture meets the in-system configuration needs of co-processor applications, in which algorithms must change in real time. Examples of these applications include wavelet compression and decompression; 27.5-MHz video compression; four-tap FIR-filter biasing; and multispectral-image enhancement. The FastMap µP bus interface lets you reconfigure the chip in less than 200 µsec. The interface configures the logic array and is configurable as 8, 16, and 32 bits wide. The chip can configure as many as 32 bits in approximately 40 nsec.

The XC6200 also features distributed memory, which means that you can use a basic cell for either logic or memory. Each logic cell contributes 2 bytes of memory. With distributed memory, a device with 16,384 cells can provide 32,768 bytes of memory. The device's fast reconfiguration capability lets you dynamically change the number of cells used as logic and the number used as memory.

Each XC6200 device comprises a large array of simple 4×4-bit configurable cells in a fine-grained architecture that implements data-path and data-processing functions for embedded control. Cells contain a function unit that can simultaneously implement a logic function and an independent routing area for intercell communication.

Device density ranges from 8000 to 64,000 gates, making the XC6200 suitable for data-path and structured-logic designs. An 8000-gate device costs $25 to $30 (10,000), and a 64,000-gate device costs $200 to $250 (10,000).—by John Gallant

Xilinx Inc, San Jose, CA. (408) 559-7778.

Circle No. 461


$50
$5
$0.5
$0.1
Cost per MFLOPS
Cost per MIPS
1982
1992
2002

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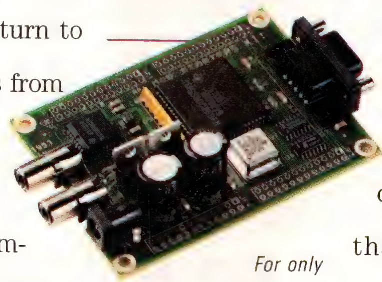
When driving toward real-time processing and cost-effective functionality at the best value, turn to Digital Signal Processing Solutions from Texas Instruments. With TI DSP Solutions, you have the raw processing power available to compress/decompress information as well as encode and decode at rates required for real-time audio and video applications. Like cellular communications, modems, multimedia audio, voice recognition, imaging and videoconferencing.



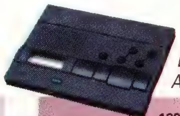
For only $99, you can get the TI 'C2x DSP Starter Kit. It offers you a low-cost, easy-to-use tool for initial understanding of TI DSP Solutions. And includes board, assembler and debugger software, sample programs and documentation.

DSP Solutions from $10 to 2 Billion Operations Per Second. Select from over 100 TMS320 DSPs that were created specifically for real-time processing. Combine them with our Mixed-Signal DSP peripherals that have optimised interfaces, I/O ports and addressing features for accessing real-world data. And you can create price/performance solutions that will help you win in today's marketplace. For example, TI has DSP and Mixed-Signal Solutions for your applications from as little as $10.*

Test-drive the TI TMS320C2x DSP Starter Kit for $99. TI DSP Solutions can help you stay ahead on the price/performance curve. For more information on the 'C2x DSP starter kit, please circle the reader service number below.

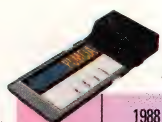
Cellular Phone

	1988	1995
Talk Time	2 hours	3 hours
Size	8"x3"x2"	5.5"x2.3"x1"
Weight	2 pounds	0.5 pound



Digital Telephone Answering Device

	1988	1995
Reliability	Tape-Based	Solid-State
Caller ID	No	Yes
Mailboxes	No	Yes



Fax Modem

	1988	1995
Baud Rate	2,400 bps	28,800 bps
Capability	Data/Fax	Data/Fax/Voice
Format	PC Half Card	PCMCIA

Hard Disk Drive

	1988	1995
Access Time	60 ms	12 ms
Size	3"x6"x8"	5.8"x4"x0.9"
Density	20 Mb	400 Mb

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CIRCLE NO. 91

DELIVERING THE HIGH-SPEED CLOCK: IT'S NOT EASY TO BE ON TIME

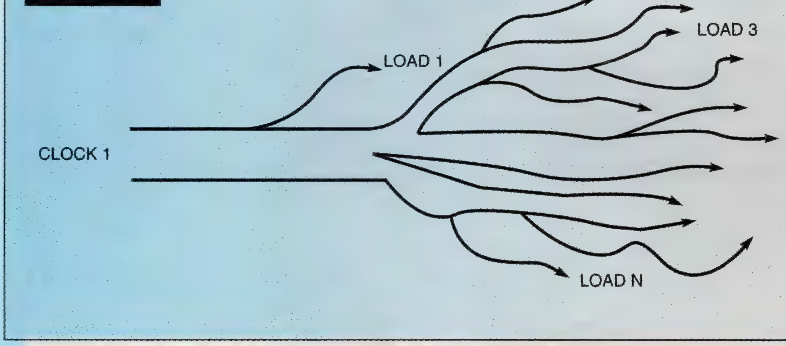
BILL SCHWEBER, TECHNICAL EDITOR

The high-speed clocks that are the pulses of today's processor-based circuits rank after dc power as the second most widely distributed signal in the system. Ironically, though, they are at the opposite end of the frequency spectrum from power. They are timing pulses—the minimal essence of digital information—but their ~100-MHz rates mean they are subject to all the vagaries of the stormy analog world.

Yet, reliable clock generation and distribution are critical in your high-performance PC or communication system. Clock-related failures are notoriously intermittent, varying with temperature, power-supply rails, internal loading, and many other hard-to-quantify factors. If your clocks aren't up to spec, you'll be chasing seemingly unrelated and irreproducible failures in the memory, I/O, CPU, and other areas.

Good clock system design is neither easy nor magical. It requires you to use basic engineering techniques carefully and thoroughly for error budgeting, worst-case analysis, verification, layout consideration, power and grounding, and minimizing noise. To these problems, add refusing to cross your fingers and hope for the best, because timing margins are too tight for you to rely on good luck. The reality is that a *statistically stable*

FIGURE 1



Signal distribution has a simple goal: to ensure that clock signals reach all ICs within a specified amount of skew.

For the digital system clock in high-speed processors, being late—or even being early—causes serious system problems. By doing your homework and not taking design risks, you can ensure that your clock edges make their transitions in the right time window.

Illustration by Gregg Dinderman

design, with guaranteed clock generation and distribution timing, is achievable: The proof is the millions of reliable PCs in use, with their relatively low soft-failure rates.

Start by mapping your needs

Keep in mind your fundamental objective: to ensure that your system's ICs get their needed clocks without waveform degradation in sufficiently close synchronization (small enough skew) with respect to each other. Start by making a clock-load inventory: what clock frequencies does your system need for which functions (memory, CPU, I/O, and so on) and locations (which ICs and where they reside)? A typical Pentium-based PC needs processor, Peripheral Component Interconnect, a floppy-drive-adapter, keyboard-controller, and system-reference clock frequencies.

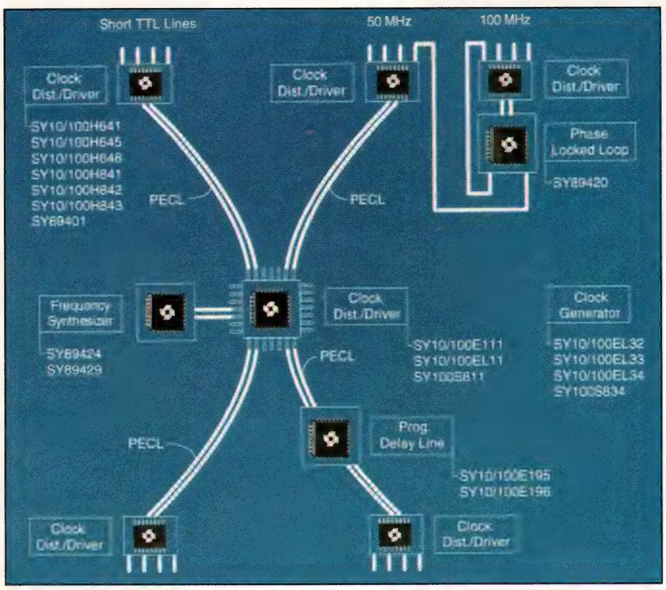
The CPU clock usually has the highest frequency in the system, but high-resolution video-display circuitry can have comparable or higher clock rates. As CPU speeds increase (**Table 1**), their designers realize that it's unrealistic to expect a more-than-100-MHz signal to reach the CPU with proper timing and integrity. Above 50 to 100 MHz, switching noise becomes a major problem. Instead, CPUs incorporate an internal PLL to multiply the supplied clock rate up to the desired internal frequency or frequencies. For example, the PowerPC 601 CPU from Apple, IBM, and Motorola internally derives its 245-MHz clock from a supplied 75-MHz clock. Result: At the cost of a little extra internal silicon, the CPU and its various subsections come with clocks, taking some of the burden off you. **Table 2** lists some representative clocks.

Your design challenge is to make sure that all clocks in the system are properly timed with respect to the CPU clock. Working against this objective are the laws of physics: Differing propagation time, or "time of flight," in each path leads to skew in signal-arrival times among the loads.

TABLE 1—PROCESSORS AND THEIR BUS-CLOCK RATES

Vendor	Processor	Clock rate (MHz)
Apple/IBM/Motorola	PowerPC	80
Digital Equipment Corp	Alpha	>100
Intel	Pentium	60, 66
Intel	P54C	99
Intel	486	66, 99
Mips	R4400SC	150

Skew is analogous to a fixed offset (see **box**, "Simple function, but unusual specs"). As long as time of flight remains constant, you can design in suitable delays to equalize it properly (deskew) in all branches. The real problem is the jitter—minute, apparently random variations in skew. Jitter comes from unavoidable variations in propagation delays due to component tolerances, power-supply and other noise, pc-board variability, and other factors. A buildup of jitter can soon overwhelm your relatively small skew-tolerance budget. Even production device-to-device variation, normally not a major concern for circuit designers, is an issue you must take into account.



The complete distribution network comprises clock sources, drivers, buffers, and delay elements, in some cases using mixed IC technologies. (Courtesy of Synergy Semiconductor Corp).

At the same time, you have to maintain signal fidelity and integrity throughout, with a clock waveform at the load that has essentially the same waveshape, including rise and fall times, slew rates, and overshoot and ringing, as it has at the source. To make matters worse, fast slew rates and sharp waveform corners also generate EMI that can affect adjacent circuit performance and cause you regulatory-approval difficulties.

Live within a budget

Once you define your system needs, work on a distribution strategy. Here's where the serious engineering work begins. You lay out a tree, branch, and leaf topology (**Fig 1**) that provides required clock signals in the right places. A large computer system can have half a dozen levels of intermediate buffering in contrast to a single-board PC, which can have just one buffer level.

You then begin work on timing analysis and error budgets, so that signals emerge from all distribution leaves at precisely the same time. Although the conceptual schematic of signal distribution goes in a "straight line" from a source through all branches to the loads, most layouts physically implement this schematic as a radial pattern to roughly equalize signal-path lengths. Eventually, you must more precisely equalize signal-path lengths, but a radial design is a starting point. Your constraint is the longest path delay for the clock; you must delay all other signals to match this time.

How much precision in the delay is enough depends on the specifications for the processor and peripheral functions. Typically, you have only a few hundred picoseconds or less of skew allowance between clocks at the various loads. Skew comes from differences in physical path lengths, as well as propagation delays within the active components. The speed of light in a

vacuum is ~1 ft/nsec (30 cm/nsec), and signal-propagation speed on a circuit board is roughly one-half that figure. Figured as a propagation delay, this corresponds to delays of 150 to 200 psec/in. (60 to 80 psec/cm).

Skew specs are tight when 1.5 nsec is 10% of a 66-MHz clock-cycle time. With the skew absorbing so much of your clock-cycle time, little timing margin is left at the load. To meet this reduced margin, you may have to use more costly 8-nsec DRAMs in place of less expensive 12-nsec devices, for example. According to **Ref 1**, you cross a threshold of significantly increased design difficulty when you have more than 10 board-level clock loads combined with a tolerance budget that is less than 10% of the clock period.

Starting the signal

A typical system needs multiple copies of each clock frequency. For a representative Pentium-class chip set, you likely need four copies of the processor clock, six of the PCI bus clock, two of the system-reference clock, and one each for the floppy-drive adapter and keyboard controller—a total of 14 clocks. A PLL-based oscillator (**Fig 2**), such as Integrated Circuit Systems' ICS9159C-02, Cypress Semiconductor Corp's CY2254, IC Works' W48C60-402, or Integrated Device Technology's IDT74FCT3907, provides all 14 signals from a single 14.31818-MHz crystal, the de facto standard crystal frequency that most PC clock ICs use.

If the PLL provides all the signals you need, then your task is relatively simple: Work out the propagation times to the loads on your circuit board without intermediate active components—the basic time-of-flight calculation. Then, determine what compensating delays you need. At these clock rates, you most likely use transmission-line techniques for interconnection on your circuit board beyond a few inches of travel to maintain signal-shape integrity and to control propagation speed.

Stripline or microstrip layout (**Fig 3**) gives a fixed-impedance path, with propagation velocities you can calculate. The actual speed is a function of the nominal speed and the load at the end of the line, so factor that in, as well. Design impedances of 60 to 70Ω are common, with signal velocity of 0.55 to 0.6 *c*.

The distribution net for a simple and common point-to-point topology looks like a set of series-terminated transmission lines driving single loads (**Fig 5**). For first-order analysis, add the propagation delays to find the slowest path and minimize sources that cause delays on the faster clock paths or speedups on the slower ones. Use the skew and clock-arrival tolerance data to

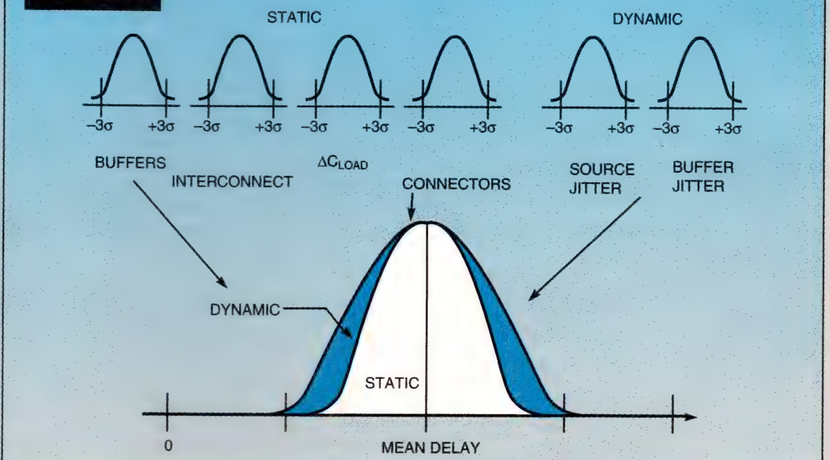
SIMPLE FUNCTION, BUT UNUSUAL SPECS

As with so many other specialities, clock generation and distribution has its own subculture of critical specs. The Joint Electronic Device Engineering Council's Standard 99 defines the following four basic types of skew for clock drivers:

- **Input skew**: the difference in propagation delay for a defined device output, originating from more than one input to the device; this skew is typically used with multiple-input gates.
- **Output, or pin-to-pin skew**: the difference in propagation delay between fastest and slowest outputs on a single device with a single input.
- **Pulse skew**: the difference between the propagation delay of the high-to-low and low-to-high transitions on the same output for a device at identical operating conditions; this skew lets you quantify the output clock's duty cycle and pulse-width distortion.
- **Process, or part-to-part skew**: the difference in propagation delay between outputs on two identical devices with a common clock under defined conditions.

Although skew is statically distributed, or time-invariant, you also must contend with dynamically distributed, or time-variant jitter. In time-variant jitter, the signal edge varies from one cycle to the next as a result of shifts in the IC's switching threshold. These shifts, in turn, are due to power and ground noise and temperature and supply variations. Jitter—a statistical broadening of the distribution of edge location—normally increases when noise increases or the edge rate of an input to a buffer decreases (**Fig A**).

FIGURE A



Jitter adds to static delays, broadening the uncertainty in clock-edge arrival time at the load.

TABLE 2—REPRESENTATIVE CLOCKS

Vendor	Device no.	Name	Description	Features
Applied Micro Circuits Corp Circle No. 315	SQ4406Q	PLL clock generator	12 outputs (three groups of four)	20 to 60 MHz out; 2x, 1x, ½x clock; each group: separate power-down; various lead/lag options
	SC3327S	10-output driver	Three outputs at input frequency; seven at one-half frequency	80 MHz, 24-mA drive, 3V, internal series resistor
	SC3368S	14-output driver	Six outputs at input frequency; eight at one-half frequency	Similar to SC3327S
Cypress Semiconductor Corp Circle No. 316	CY2291	Three-PLL clock generator	Eight outputs: four fixed, four configurable	Factory EPROM custom-rate versions, 30 frequency options, selectable shutdown, smooth ramping from 4 to 100 MHz
	CY7B9910 (TTL), CY7B9920 (CMOS)	Low-skew clock buffer	Generates eight copies, PLL for low skew 1	5 to 80 MHz; 250-psec skew, 500-psec propagation delay, 1-nsec device skew
	CY2254	Pentium clock synthesizer/driver	14 clock outputs: four CPU, six PCI, one floppy, one keyboard, two reference	3.3V, 200-psec jitter, 200-psec skew (CPU clocks), 500-psec skew (PCI clocks)
IC Works Inc Circle No. 317	W42C27	CPU-frequency generator	Dual output for Pentium and PCI bus	3.3 or 5V, also supports Fibre Channel-Arbitrated Loop with 106.25-MHz output
	W40C06A	Six-output buffer	DC to 66 MHz, each output drives one or two 50Ω lines	3.3 or 5V supply, integral oscillator, 48-mA drive
	W48C60-402	Pentium/PCI bus synthesizer	14 clock outputs: four CPU, six PCI, one floppy, one keyboard, two reference	3.3 or 5V operation
Integrated Circuit Systems Inc Circle No. 318	ICS9159C-02	Clock generator and integrated buffer	14 clock outputs: four CPU, six PCI, one floppy, one keyboard, two reference	100 MHz (5V) or 66 MHz (3.3V), CPU- and bus-clock rates separately selected
	ICS9178-02	Frequency-timing generator for Power PC	14 clocks: two 2x PECL CPU, one TTL CPU; 10 selectable bus	5V: 75 to 245 MHz, 3.3V: 60 to 170 MHz
	ICS9159-07	Frequency-timing generator for NexGen Nx586 CPU	13 outputs: three CPU, seven PCI, one reference, one floppy, one keyboard	Smooth frequency transition for green operation, choose nine clock rates, 65 MHz
Integrated Device Technology Inc Circle No. 319	IDT74FCT3907	PC-clock synthesizer	14 clock outputs: four CPU, six PCI, one floppy, one keyboard, two reference	3.3V, pin-selectable CPU clock at 50/60/66 MHz, 200-psec skew (CPU clocks), 500-psec skew (bus clocks)
	IDT74FCT3932	PLL-based CMOS clock driver	17 three-state outputs: four, eight, five/bank	3.3V, 16 programmable frequency configurations, up to 100 MHz
	49FCT805T series	Low-skew clock driver for datacomm	Dual 1-to-5 output multiplexer	TTL input/output; 3.3, 5V versions; selective shutdown; inverting, noninverting versions
Micro Linear Corp Circle No. 320	ML6500	Programmable adaptive clock manager	PLL clock, eight outputs	Adaptive deskew buffers via feedback, 10- to 80-MHz range, 5-nsec deskew range
	ML6510	Programmable adaptive clock manager	PLL clock, eight outputs	Deskew via reflected waveform; to 130 MHz; 3, 5V outputs
	ML65244	Dual/quad-buffer line driver	Two groups of four outputs	TTL compatible, 1.5-nsec propagation delay
Motorola Inc Circle No. 321	MC100LVE111	Low-voltage one- to nine-line clock driver	Differential input and output, ECL/PECL	50-psec output skew, 75Ω pulldown resistors
	MPC950	Low-voltage PLL clock driver	Nine output, crystal or external reference	Outputs to 250 MHz, output skew 350 psec
	MPC974	PLL clock driver	15 outputs (Three banks of five each)	Can switch between two source-reference clocks' output ratios 1-to-1, 2-to-1, 3-to-1, 3-to-2, 3-to-2-to-1
National Semiconductor Corp Circle No. 322	CGS74CT2524 family	One to four fan-out clock driver	Family of four devices, 300-psec output skew	5V operation, 24-mA drive, eight-pin package; CGS74LCT2524 series is 3V, 12-mA output
	CGS700	PLL 1-to-9 CMOS clock driver	Fan-out of 9	25 to 160 MHz; 30-mA drive; outputs at 1x, 2x, 4x reference, internal loop filter
	CGS2534V family	Quad-memory-array clock drivers	Four inputs, 16 outputs, to 125 MHz	Various inverting, noninverting combinations; output structures, two output (CGS2536)
Quality Semiconductor Inc Circle No. 323	QS5917T-70T, -100T, -133T	CMOS PLL clock driver	Four outputs: Q0-Q4, 2xQin, Qin/2, Q5	Integral loop filter, 70/100/132-MHz clock; 24-mA output drive
	QS5805T, QS52805T	CMOS clock driver/buffer	10 outputs: five inverting, five noninverting	5V, 5280x series has 25Ω series resistor for driving unterminated lines
Synergy Semiconductor Corp Circle No. 324	SY89424	Frequency synthesizer	PLL-based, single-output clock to 1 GHz	12.5 to 25 times crystal frequency, selectable
	SY10H842	PECL to TTL one- to four-line clock driver	Single PECL input to four TTL outputs	24-mA output, 1-nsec pin skew, TTL, PECL grounds
	SY10E195	Programmable delay line	2-nsec range, 20-psec steps	Can be cascaded to increase delay range, E196 has analog input for finer resolution
Texas Instruments Inc Circle No. 325	CDC586, CDC2586	3.3V clock driver	12 outputs, up to nine can be selected to run at one-half or two times input frequency	50 to 100 MHz, CDC2856 has internal 26Ω resistor, TTL-compatible inputs and outputs
	CDC351, CDC2351	3.3V, one- to 10-line clock driver	Distribute clock to 10 outputs	32-mA drive, low-voltage-TTL-compatible, output enable control, CDC2351 has internal 26Ω resistor

Price
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$3 (10,000)
$3.50 (10,000)
$2.28 (10,000)
$4.95 (10,000)
$3.10 (10,000)
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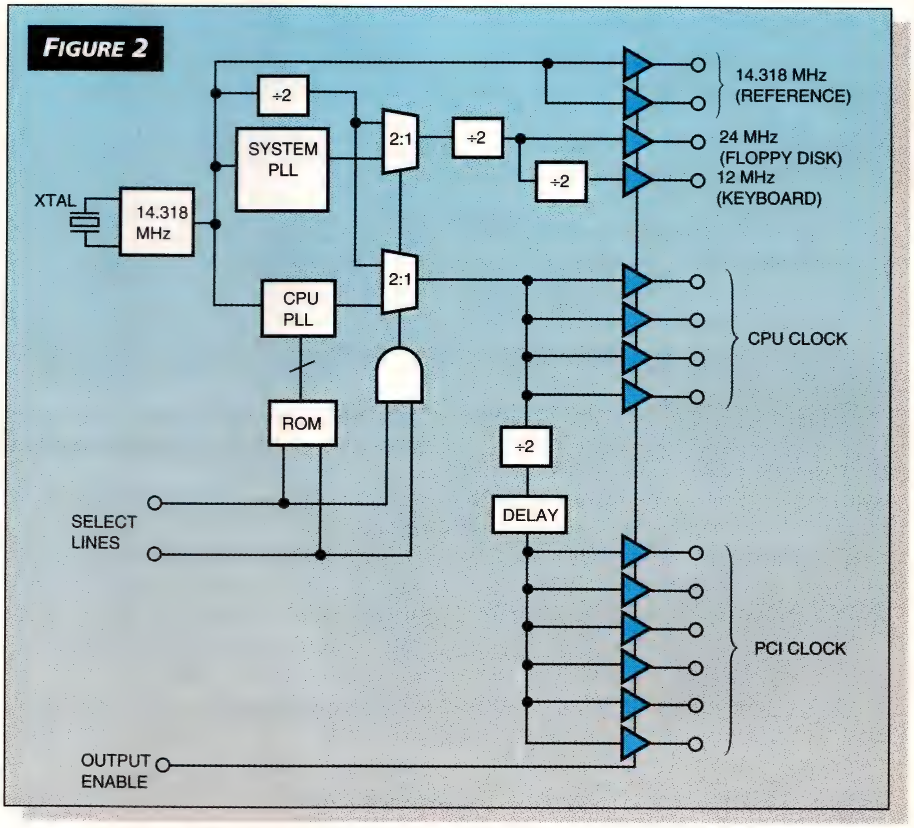
$5.35 (1000)
$9.25/$11.57/$1388 (1000)
$5.74/$6.72 (1000)
$17.85 (1000)
$8.75 (1000)
$18.45 (1000)
$8.84 (1000)
$4.02 (1000)

FIGURE 2



From one crystal, a single PLL can provide all necessary clocks for a PC chip set.

determine your maximum allowable jitter, as follows:

tolerance≥intrinsic skew+extrinsic skew+jitter

or

jitter<tolerance–intrinsic skew–extrinsic skew.

IC data sheets and specifications for the various loads provide tolerance data and intrinsic output skew. For example, the Pentium specification requires that the clock difference between the CPU and the cache controller be less than 200 psec, and timing between other system functional blocks has similar specifications. Extrinsic skew comprises the sum of variations in the propagation delay of a signal through a loaded transmission line with various loads plus tolerances in the interconnect due to manufacturing variations. Rise and fall times typically slow by 0.5 to 1 nsec per 10 pF for 10- to 50-pF loads. Typical values for interconnect tolerances range from 1 to 50 psec/in. times the length of the interconnect. **Ref 1** provides the formulas and IC-vendor application notes.

Buffers, PLLs offer choices

Once you design your clocks, the real challenge begins. Whether you need more clock copies, clock regeneration for signal integrity, or distribution across a multiboard system, you have two choices: a buffer or a PLL. Each has advantages and shortcomings. You may carefully mix both in a system for the best performance, cost, and reliability trade-off. Also, analyze whether a signal driver should drive more than one load. Point-to-point layout requires more buffers or PLL outputs than using one driver for multiple loads. However, point-to-point layout minimizes tolerancing from variations in load capacitance. Load variations cause timing variations, which increase as the number of loads on a driver increases.

Buffers tend to be lower cost and easier to use than PLLs. A single multichannel buffer can handle different

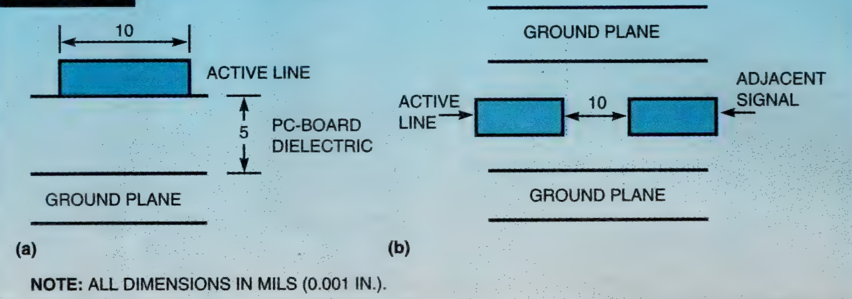
clock signals, thus easing board layout; many buffers allow you to parallel their outputs for increased drive. In addition, some buffers, such as Applied Micro Circuits Corp's SC3368S, National Semiconductor Corp's CGS2536V, and Texas Instruments Inc's CDC586 family, also provide basic divide-by-2 functions for a half-rate output, which is useful for some systems. As "digital" functions, buffers are somewhat more resistant to supply-rail noise than are PLLs with their closed-loop operation.

Buffers have their drawbacks, however. For example, they have both propagation delay and jitter in the delay. They also have part-to-part and channel-to-channel differences. They also can provide only copies or half-rate versions of the input, so that you need a buffer for each clock frequency.

PLLs offer two features that simpler buffers lack. Due to a PLL's phase-locking servomechanism, the PLL produces a synchronized original rather than a mere regenerated copy, and its output has zero delay with respect to the input. Some PLLs allow you to add some calibrated delay to compensate for delays elsewhere. In addition, PLLs can use internal dividers to produce outputs that are multiples and submultiples of a master clock, and these other clocks can be in noninteger ratios from the master.

PLLs can also help when you don't have control of critical-path signal timing. For example, final timing specs for an ASIC may not be available until relatively far into the design cycle. Fortunately, a PLL can effectively minimize within a broad span any timing error in the ASIC.

FIGURE 3



Stripline (a) and microstrip (b) trace layouts give you characterized impedance and propagation delays; typical dimensions are shown.

Despite these virtues, PLLs bring new concerns. For example, noise on their supply rails and inputs affects PLLs more than it does buffers. Because PLLs have active, closed-loop functions, this noise and other noise, such as crosstalk, can cause "noise multiplication," unanticipated modes of interaction and unexpected spectral components. Application of PLLs requires both designers and IC vendors to have a thorough understanding of the devices' dynamics and characteristics.

Although using multiple PLLs in a large system seems to solve many problems, such as the need for zero delay and multiple clocks, subtle interactions can develop between the PLLs, especially when their bandwidths are incompatible. Keep power rails clean and keep noise out. Achieving these goals requires good filtering, bypassing, and grounding. Use local power regulation in areas in which you anticipate that passive techniques will not suffice.

Collect the facts

Whether you do your initial analysis with pencil and paper, a spreadsheet, or electronic-design-automation modeling tools, you need timing data. (See box, "Tools and models offer help—with limitations.") Manufacturer data sheets are vital not only for basic timing specs, but also for information about delays and jitter within an IC and all production units of the IC. Here's where you have to be careful: Check on the quality of this data by looking at test reports. Determine whether specs are based on samples of a few or many production units. Identify which sampling techniques the manufacturer uses for maximum and minimum specs. Find out whether the devices come from related or unrelated production lots and what defines an "unrelated" lot. Determine how the

VERIFYING YOUR RESULTS

You've built a circuit board that works. But, postpone your celebration until after you verify that the design is statistically stable. Your initial analysis is important in developing a confidence level with a working design because you have to know what timing variations will emerge and where to expect them. Then, you have to simulate these variations with injected signals. Many buffers allow you to put their output into high-impedance, three-state mode to ease signal injection at critical points in your distribution system.

As in all testing, the accuracy and resolution of the test instrumentation must be better than the system under test, typically by a factor of 10, to provide meaningful results. This limit is a challenge when you're working in the picosecond range. Instruments such as the HP 8133A 3-GHz pulse generator provide less than 1.3-psec rms jitter and about 8-psec worst-case jitter—well within the typical 50-psec Pentium tolerance budget. The HFS 9003 data generator from Tektronix can generate pulses with rise times as low as 250 psec and edge placement accuracy to 5 psec. A 1-GHz or wider bandwidth sampling scope checks clock-waveform timing, including rise time, jitter, and skew, as these signals reach the ICs in your system.

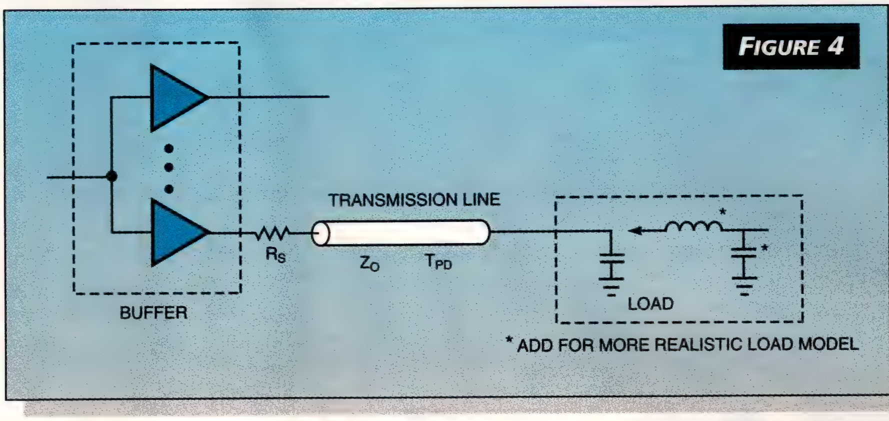
manufacturer chooses the samples and how it distributes the data. Review the basics of statistics and reliability analysis, not to find out whether these ICs will fail catastrophically, but to better understand the meaning of the datasheet numbers.

Although you must design for worst-case situations, overall error buildup is not necessarily just the sum of the unrelated individual worst-case error values. Such simple addition may inadvertently indicate the need for tighter tolerances or faster memory ICs or suggest a system that may work unreliably. Variations in skew may occur as ICs slow down or speed up with temperature decreases and increases. This correlation may give you some more tolerancing, following careful analysis of the basic data.

Due to the unavoidable path-length and propagation delays in some clock branches, you must add some compensating delays in other branches. You can use both passive and active approaches, as long as you recognize their trade-offs. The simplest approach is to add some circuit-board tracks to lengthen the faster paths. You can easily calculate the lag time through these apparently free, "serpentine" delay elements, especially if you use transmission-line techniques. These techniques are also reliable, power-supply-independent, fairly repeatable, and relatively low jitter compared to active devices.

Unfortunately, even modest delays

FIGURE 4



The simplest distribution model has a series-terminated transmission line driving a single load.

LOOKING AHEAD

It's logical to predict that the future will bring more 3V clocks, faster clocks, and clocks integrated with the CPU, following the trend of most other electronics. But only the first item is likely. Clock ICs employ processes that can run two to three times faster than most current ICs need to, and some clocks do, such as the 267-MHz Rambus clock. Weighing against that trend, however, are the difficulties and design cost of putting clocks on CPU silicon and of properly distributing clocks that are faster than the current 60 to 100 MHz.

Integrating the clock with the CPU is difficult, because the frequency requirements and fan-out differ among system implementations. A low-jitter, tightly controlled clock is hard to integrate on CPU silicon and entails subtle problems in final silicon implementation that would delay the CPU's release to customers. IC-design and electronic-design-automation tools for clock subsystems differ from and are not as exact as those for CPU logic. In addition, your system's need for multiple clock frequencies and their copies would mean a greater increase in package size and pin count than the CPU and its package can afford. A single clock line from the CPU would still need an external buffer for multiple loads and timing control, so the benefit of an integral clock source may be less than it seems, especially if the CPU IC clock lacks some of the features of stand-alone clock ICs. Finally, physical placement of the clock is critical, and placing it at the CPU reduces the flexibility in location that noise and grounding may demand.

Today's 486- and Pentium-based chip sets have reduced chip count and, consequently, need fewer clock copies and are well-served by integrated generators/buffers. In contrast, PowerPC and RISC chip sets are less condensed. Clock vendors are tailoring their efforts to provide the clock frequencies and distribution for these families. They're also expanding beyond today's clock frequencies. Clock generators will emerge that provide some of the clock frequencies PCs require. There are yet *more* clocks within PCs for such functions as multimedia.

For example, Integrated Circuit Systems' ICS9120-08 series uses the standard 14.31318-MHz CPU clock crystal to provide standard audio clocks at 16.9344, 25.576, and 33.868 MHz. Oversampling codecs and audio synthesizers in PCs use these values. Despite the relatively low frequencies compared with the processor clocks, good audio performance (16- to 18-bit sound with –96-dB S/N ratio) still requires tightly bounded specs. The IC outputs have 0.01% frequency accuracy and 85-psec, 1σ jitter.

High-speed clocks are not just for PCs. Data-communications systems that derive clocking from the incoming data stream must provide a retimed and regenerated clock signal to the decoder. The frequencies for these systems are often faster than those for PC clocks, and jitter specs are correspondingly tighter, but fan-out needs are less. Clock-IC vendors are adapting their technologies to these applications and to video-compression and -decompression systems that operate at several hundred megahertz.

In addition, some computer researchers are investigating the benefits of fully or partially *clockless*, asynchronous CPUs, which might use far less power and have simpler internal circuitry than fully clocked, synchronous devices (**Ref 6**).

HIGH-SPEED CLOCKS

cost significant circuit-board space, which is generally a precious commodity. Each nanosecond requires approximately 6 in. (15 cm); even a few nanoseconds of delay in each of several branches can quickly consume board space. Any layout changes in your circuit also require recalculation of the serpentine traces and are another constraint on flexibility. Moving the clock-generation and distribution ICs may help, but most circuit boards have local-noise hot and cold spots. Don't make such moves casually.

In the active approach, you can choose delay lines, such as the Synergy SY10E195. Carefully check the stability and repeatability of these adjustments, or you may add jitter uncertainty while correcting for skew. Any compensation scheme is costly if your clocks have a large fan-out. Another approach is to reduce delay by replacing a buffer with a PLL and recalculating system errors and costs.

With so much concern about static delays and dynamic timing issues, another approach is to use adaptive techniques to dynamically adjust clock-signal timing. Micro Linear Corp offers ICs that provide two approaches to adaptive timing. The eight-channel ML6500 clock manager uses a feedback trace from each load, which the driver uses to measure the timing of the pulse at the load and make necessary vernier adjustments. This approach offers a degree of freedom in handling dynamic errors, but it costs an additional trace per clock line.

The ML6510 takes a different approach. It automatically determines the length of the trace it is driving by measuring the time for reflections to return from the end of the trace. The driver then adjusts a voltage-controlled vernier delay that sends the clock earlier in proportion to the length of the trace. Regardless of which adaptive technique you use, make sure that the overall deskew range, resolution, and stability are sufficient for your circuit.

Low voltage offers benefits

As in many other areas, designers are increasingly mixing 3 and 5V devices to reduce power consumption. This technique also eases IC-driver design and EMI concerns. Lower signal spans have lower noise margins, however, but this is not a major problem. For mixed-voltage systems, vendors provide buffers that operate from a 3V supply and that accept 3 and 5V signals.

For "green" or mobile systems, you may need to slow the clock or put it into a power-down mode. Sounds simple, but make sure that your clock is well-behaved when it accelerates to full speed. If the clock ramp-up is not smooth or too rapid, the CPU may lock up when the clock first appears at the wrong time during the transition sequence. Many newer clock-generation ICs guarantee smooth acceleration.

Reducing EMI is always an issue. Radiated signals can affect other parts of your system and produce external interference. Faster slew rates reduce clock skew and jitter, and lower slew rates minimize EMI. Fortunately, vendors shape driver outputs so that the necessary fast slew rates begin and end with rounded corners. These waveshapes meet signal-transition specs and reduce sharp corners and their corresponding broad signal spectrum.

Clock generation and distribution is a single-supply circuit. To accommodate speeds beyond the range of TTL, clocks often use positive-ECL (PECL), which uses a 5V supply. Vendor application notes give details and equations

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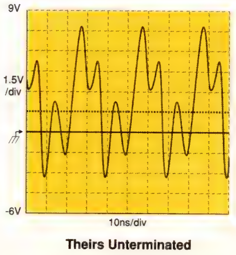

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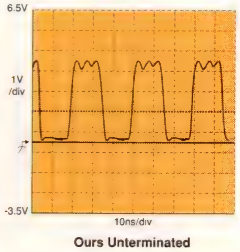

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Calling for help can't hurt

In this specialty area of clock-timing and -distribution ICs, where "perfect" digital signals meet the real analog world, take advantage of IC vendors' application departments. Their experience can shorten your design cycle and minimize your following paths that lead to nowhere. Some vendor-independent consultants also specialize in design, analysis, and verification of high-speed clock-generation and -distribution subsystems.

You must also decide whether to fine-tune each system. Adjusting each unit in production to minimize error sources and assure operation can save on parts cost and up-front design time—a viable alternative if you are building only a few units. It can be a costly decision in a higher volume environment, however. Besides the sophisticated test and adjustment effort in the production cycle, it means that units in the field may be unreliable if they ever have a component or subsection replaced—unless the field-repair site can also do a tune-up, which is unlikely. Your products may develop a reputation for being difficult to fix if replacing a part induces new errors or soft failures or requires a complex procedure.

However, such per-unit tuning shouldn't be necessary. If you properly and thoroughly perform your analysis and take no short cuts, you should be able to produce and verify a reliable system that works by design rather than individual unit adjustment (see **box**, "Verifying your results"). EDN

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TOOLS AND MODELS OFFER HELP—WITH LIMITATIONS

Sending well-defined, absolutely periodic digital signals around a circuit board should be compatible with modeling and analysis tools. After all, you perform no "signal processing" on the clock signal, but simply pass along or recreate the signal. Although tools can help, they have limitations. Simple tools give you a good start: Even a spreadsheet is helpful as you investigate error budgets and tolerances for vendor parts and basic topology configurations.

The next step up from spreadsheets is to use Spice models. Virtually every vendor supplies these, and they are useful for a basic, first-level check. Most models represent the load with more fidelity than does an input capacitor, by using a π configuration of the input pin with a parallel capacitor, a series inductor, and another parallel capacitor. The models also assume you are using circuit-board-transmission microstrip or stripline as your signal conduit, which you can model simply, ignoring crosstalk, or with more complexity. If the device models reflect only typical operating specs, they are little better than using a spreadsheet, because jitter deviations and worst-case conditions are your true foe.

Your problem is not analysis of signal processing or signal content on pins of complex-function ICs, however. Focus instead on signal timing and integrity on those paths related to that function. Tools for this application can help if you accept their limitations (**Ref 3**). If Spice models are unavailable or insufficient, consider using models developed under the I/O-buffer information specification (IBIS) standard (**Ref 4**). IBIS concentrates on current-vs-voltage characteristics, rise and fall times, and similar behaviorial modeling. Spice models, on the other hand, are summaries of transistor-level models and may reveal proprietary internal details that vendors don't want outsiders to know.

Don't worry if you can't model the signal path as fully as you may think is necessary, taking into account crosstalk and signal reflection. Following the guidelines for good design will take you and your signal a long way toward the goal (**Ref 5**). For example, 50Ω microstrip lines have less than 3% coupled near-end noise when the spacing to the next adjacent track is equal to the trace width; for striplines, the corresponding rule is that spacing should be at least 1.5 times the trace width.

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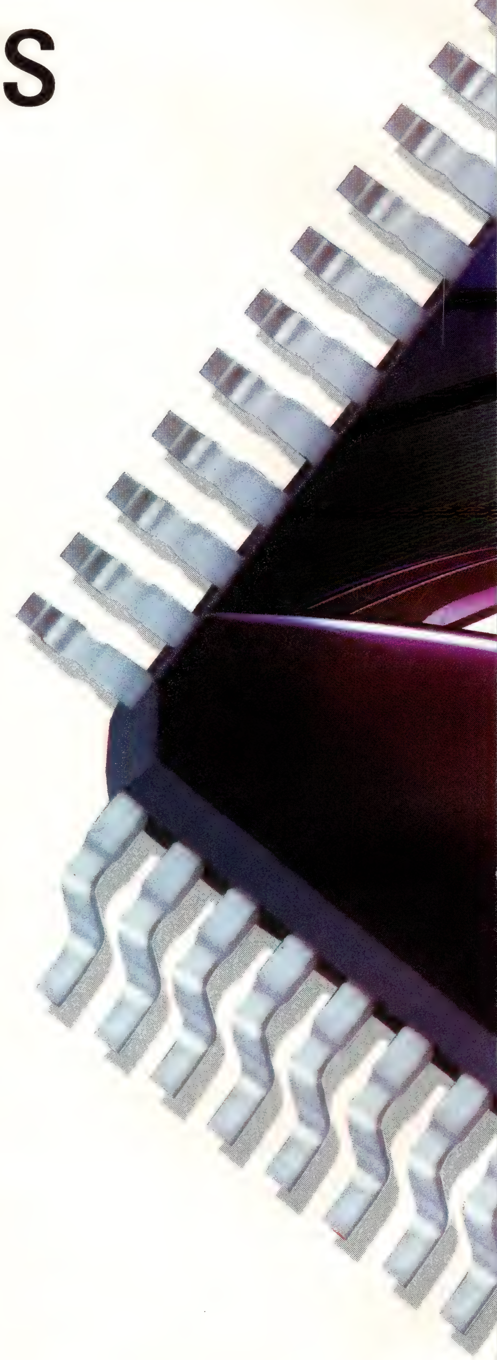

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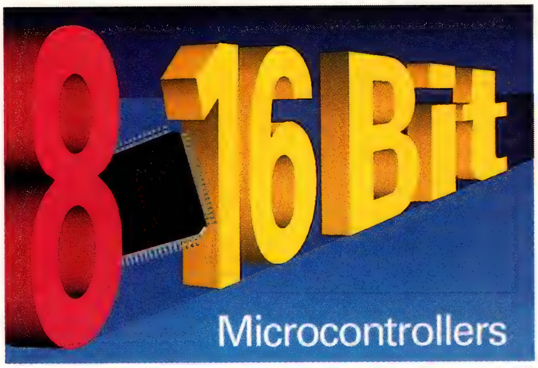

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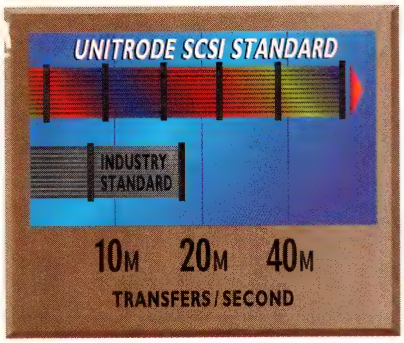

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PORTABLE HARDWARE MAKES EXPERIMENTS INTERACTIVE

Bringing the data-acquisition system to the experiment can provide useful results in a hurry. But, if you're not careful, subtle flaws in what should be invisible software can stymie your hardware installation.

DAN STRASSBERG, SENIOR TECHNICAL EDITOR

Using a notebook PC for data acquisition can alter your whole concept of experimentation. What was a tedious, iterative process becomes a dynamic, interactive one. When the same PC that controls data acquisition reduces the data and displays the results, you can learn immediately what happens when you change test conditions.

Until recently, though, bringing a PC to an experiment more than a few feet from your lab bench was, at best, inconvenient. Despite the existence of notebook PCs, virtually the only portable PCs that could acquire data at speeds faster than about 5k samples/sec were "luggable" ac-powered units weighing over 20 lb.

Data-acquisition products designed for notebook PCs began to appear about two years ago. Some of these products are external units about equal in size to the PCs themselves; others are credit-card-sized PCMCIA cards that plug into slots on the side of most modern notebooks.

Software kinks plagued early PCMCIA data-acquisition cards. Vendors have resolved many of the problems, and data-acquisition is preparing to join the portable-electronics revolution. Competition is heating up; different companies' products often look quite similar. But don't be fooled. To find hardware and software that play together well, ask pointed questions and pick vendors that supply good answers. (See **box**, "PCMCIA: A little caution saves a lot of grief.")

Nearly all PCMCIA data-acquisition cards are the 5-mm-thick Type II size. Most notebooks accept two Type II cards. Generally, the specs of PCMCIA data-acquisition cards don't quite equal those of similarly priced boards for desktop PCs, but many cards compare well with portable data loggers that lack the processing power to reduce

Signal termination and conditioning are as much a part of data acquisition as A/D and D/A conversion and translation of relay-contact status into logic levels. Strawberry Tree's DataShuttles (from $995) represent a class of parallel-port attachments that handle the full spectrum of data-acquisition-system functions.

data. The "For free information..." **box** lists vendors of PCMCIA data-acquisition cards and of external data-acquisition attachments that connect to notebook-PC parallel ports.

Small size, big features

Most analog-input PCMCIA cards have 16 single-ended inputs (eight differential) with software-programmable gain and four unipolar or bipolar full-scale ranges from ~1 to 10V. Resolution is 12 bits. Triggering can come from software or from an external source. The cards usually also offer four to eight digital I/O lines and a counter/timer. A/D-conversion speeds start at 30k samples/sec. Most vendors offer models that take 100k samples/sec, although a few run faster; the top speed is currently 140k samples/sec. A few cards provide 16-bit resolution. Some cards accept low-level (10-mV full-scale) inputs. Some even provide cold-junction compensation for thermocouples.

Only a few analog-input cards also

PCMCIA: A LITTLE CAUTION SAVES A LOT OF GRIEF

When you plug a PCMCIA card into a PC, you set in motion a chain of events that you aren't even supposed to notice. Indeed, if everything works as intended, you won't be aware of the complex drama that the PCs' hardware and software are playing out. Unfortunately, the script is quite complex, and its many plot twists and subplots can confuse the actors. Sometimes, they forget their lines. However, if you think of yourself as the director and exercise a little care at the outset, you can keep the finale from resembling the last act of *Hamlet*.

Begin by becoming acquainted with the cast of characters. Among the key players are software modules called "socket services" (SSs) and "card services" (CSs), which reside on the PC's hard disk and load into RAM at boot time. Most notebooks shipped in the past 18 months have PCMCIA V2.0 or 2.1 SSs and CSs on their hard disks. SSs act as a driver for the ICs on the motherboard that interface with the PCMCIA sockets. CSs begin to act when you plug in a PCMCIA card (or when you power up a system with a PCMCIA card plugged in), but CSs do not work alone.

Another member of the cast is a software module called a "generic enabler" (GE), or "super client." The company that supplies the GE, usually the PC manufacturer, customizes the GE for the PC's hardware. GEs for similar but not identical PCs from the same manufacturer can differ from each other.

Most vendors of PCMCIA data-acquisition cards provide a hardware-specific driver for each card. You install this driver by running an installation program that the card vendor supplies. Sometimes, this driver is part of a set of drivers constituting a dynamic-link library (DLL) that one or more Windows-based data-acquisition application packages use. This is the case, for example, with the NI-DAQ driver set that National Instruments furnishes with LabWindows/CVI and LabView. Sometimes, the DOS Autoexec.bat file installs the driver each time you boot the PC.

The application contains a driver, too

In most cases, there is yet another driver. It is part of the data-acquisition application or application-development package. Examples of such packages are TestPoint from Capital Equipment Corp (Burlington, MA), DT-VEE from Data Translation, Snap-Master from HEM Data (Southfield, MI), Visual Designer from Intelligent Instrumentation, Labtech Notebook from Laboratory Technologies (Wilmington, MA), LabView from National Instruments, and DasyLab from NewWorld Resources (Amherst, NH).

Suppliers of PCMCIA data-acquisition cards offer a variety of devices for terminating the field wiring from transducers and other signal sources found in data-acquisition setups. This unit from Intelligent Instrumentation includes cold-junction compensation for up to seven thermocouples.

Often, the application driver is not specific to a card but is general enough that an application you write for, say, an ISA bus board can run unmodified on a PCMCIA card. However, to get an application to run with specific hardware, you must configure the application to talk to the correct hardware-specific driver or the correct portion of a DLL driver set.

The proponents of PCMCIA describe the bus as "plug-and-play," which it is if everything works correctly. But, even when everything works correctly, a PCMCIA data-acquisition card doesn't necessarily work in both of a notebook PC's PCMCIA slots (or *all* slots on units that have more than the usual two Type II slots). Usually, you must configure the application software to look for the card in the correct slot. Data Translation has gone to great lengths to make sure that the software that supports its PCMCIA cards automatically recognizes the cards and properly supports them wherever you plug them in.

provide DAC outputs. You can buy cards whose primary function is DAC output, however. Some of these cards combine DACs and digital I/O lines, Other cards that lack analog inputs offer several counter/timers and digital I/O lines (24 are typical). Prices range from under $200 for purely digital cards to almost $700 for a 16-bit, eight-channel, 50k-sample/sec, analog-input card. Prices of 12-bit cards range from just under $300 to almost $600.

Although PCMCIA cards represent the current state of the art in miniaturization of PC-based data-acquisition hardware, other types of notebook-PC data-acquisition equipment do exist. Units that connect to RS-232C ports date back to the days of minicomputers. There are scores of vendors and models, but no RS-232C unit operates any faster than the serial port to which you connect it. At 115.2 kbps—very fast for an RS-232C port—a unit can transmit no more than 7.66k 12-bit samples/sec. Most units are much slower, although a few capture data bursts at

Now that we've met the players, we can try to follow the action. When you plug in a PCMCIA card or power up a PC with a card already plugged in, the GE, working in conjunction with CSs, attempts to identify the card. Identification consists of determining the manufacturer, the card function, the specific card type, and the resource requirements. These requirements include interrupt lines as well as the base address and the range of addresses in the PC's I/O space that the card uses to communicate. In most cases, after properly determining the resource needs, the GE and CSs leave the scene and let the card manufacturer's hardware-specific driver interface with SSs.

A case of mistaken identity

Complications often arise, though. In many cases, the GE causes CSs to misidentify the PCMCIA card. In such cases, the card vendor's driver must try to persuade CSs to determine the resource requirements again—this time, correctly. The alternative is to override the GE and use resources designated in the hardware-specific driver. The problem with this approach is that it can lead to some of the difficulties that were common with card-specific enablers (CSEs), the predecessors of CSs and SSs.

CSEs, which came from either card or PC vendors, allowed you to run one or a few types of PCMCIA card. CSEs' most notable problem was that their installation often caused some PCMCIA cards that once worked to stop working. Particularly under DOS (which, unless modified, does not support memory beyond 640 kbytes), CSEs would sometimes use so much memory they could keep you from running applications that ran before you installed the CSE.

The last part of the drama unfolds when you unplug a card. Whenever a PCMCIA card is in a PCMCIA socket, it connects several pins, thereby holding one of the I/O lines at ground potential. When you remove the card, a resistor pulls this line toward V_{CC}. The support chips in the PC detect when this line goes high and generate a signal indicating that the card is no longer in place. SSs then start a sequence that informs the operating system and any running applications that the card is no longer present.

Before you buy, do this...

To improve the chances that a PCMCIA card will work as advertised in your PC, do the following before purchasing a card:

- Find out if the card vendor *knows* that the card works in your PC. Knowing involves more than just guessing. If you haven't yet purchased the PC, see if you can get the card vendor to provide a list of PCs known to work with the card vendor's cards.
- Remember that the PC vendor's name and model name may *not* adequately identify the PC to the PCMCIA card vendor. Be prepared to supply the card vendor with additional information, such as whether the PC vendor preinstalled SSs and CSs on the PC.
- Know the name of the BIOS vendor, the BIOS revision number or revision date, and the name of the vendor of the PC's PCMCIA chip set. If the PC's documentation doesn't provide this information, you may have to get it from the PC manufacturer's technical-support department.
- Use a version of SS that supports your chip set. Because PC vendors customize SSs for PCMCIA chip sets, turn first to the PC's manufacturer (not to the publisher of CSs and SSs) to obtain CSs and SSs.
- See if the card vendor will send you software to test the PC for compatibility if the card vendor isn't sure that the card and the PC are compatible. Ideally, you shouldn't have to pay for this software. Data Translation provides such software free.
- Alternatively, see if the card vendor will sell you the card with a money-back guarantee. That is, if you can't make the card work, the vendor provides a return-material authorization, you return the card, and the card vendor does not bill you.
- When you unpack the card and complete the software installation, make sure that applications that ran previously still run and that other PCMCIA cards that worked previously still work.
- Make sure that the driver in your data-acquisition application or application-development package interfaces correctly to the PCMCIA card vendor's hardware-specific driver. If you buy the card and the application software separately, make sure that each of the vendors *knows* that the drivers are compatible.
- Don't assume that using a "name-brand" PC precludes problems or that using a little-known brand of PC invites trouble. One PCMCIA data-acquisition-card vendor supplied *EDN* with a list of over 140 PCs. The list includes PCs known to work with the vendor's cards, PCs that don't work, PCs that probably work (but haven't yet been tested), and PCs that may not work. The size of a PC's manufacturer appears unrelated to the PC's degree of compatibility with this vendor's cards.

high speed and store them internally for serial transmission to the host PC.

Table 1 compares the speed of several buses and ports that can connect data-acquisition devices to PCs. The **table** indicates the bus or port speed, not the speed of the data-acquisition hardware (the ADC, for example). Moreover, most data-acquisition units resolve 12 or 16 bits. Transferring a single reading usually takes 2 bytes. (A 12-bit unit *could* transfer two readings in 3 bytes, but few do so.)

Many PCs introduced in the past year have an enhanced parallel port (EPP) rather than a standard (Centronics) port. Data-acquisition units designed to connect to Centronics ports work equally well with EPPs. The EPP is backward-compatible with the two-decades-old Centronics standard but offers better two-way communication and is faster when operating with equipment designed to take advantage of its speed.

TABLE 1— BUS AND PORT SPEEDS

RS-232C	11.5 kbytes/sec
Standard parallel port	180 kbytes/sec
EPP	800 kbytes/sec
IEEE-488	1 Mbyte/sec (faster with short cables or special implementations)
PCMCIA	1.5 to 2.5 Mbytes/sec
ISA bus	2 to 2.5 Mbytes/sec (depends strongly on the PC)

Note: Most cards use 12- or 16-bit ADCs, so one reading usually takes 2 bytes, although it is technically feasible for software to pack two 12-bit readings into 3 bytes. (Data courtesy of IOtech)

Faster than a speeding ADC

The speeds of the EPP, the IEEE-488 bus, and the PCMCIA bus fall in a range of about 3:1. Unlike RS-232C and Centronics ports, these ports and buses are faster than most of the data-acquisition units you can connect. For example, despite the PCMCIA bus's 2.5-Mbyte/sec maximum transfer rate, only a few PCMCIA ADC cards acquire more than 100k samples/sec.

Similarly, when connected to EPPs, nearly all parallel-port data-acquisition units that were designed to take advantage of EPP speed run only as fast as their ADCs allow. The EPP is faster than 12- or 16-bit ADCs with a top speed below 350k to 400k samples/sec. When you use a Centronics port to connect a unit designed for the EPP, the unit functions but runs more slowly than it does on an EPP.

Many parallel-port units replicate the PC's printer port. Therefore, you don't have to disconnect the data-acquisition unit to connect a printer. The data-acquisition-unit driver intercepts messages intended for the printer. Before passing those messages to the PC's parallel port, the driver sends signals through the port. These signals stop data acquisition and make the external unit echo to the printer any signal from the PC and echo to the PC any signal from the printer.

Vendors of parallel-port data-acquisition attachments include Dataq, IOtech, Intelligent Instrumentation, National Instruments, Omega, and Strawberry Tree. Prices for units with eight differential analog inputs and 12-

FOR FREE INFORMATION...

For free information on the notebook-PC data-acquisition products discussed in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use *EDN*'s Express Request service. When you contact any of the following companies directly, please let them know you read about them in *EDN*.

Notes:
C=Supplies PCMCIA data-acquisition cards.
E=Supplies external data-acquisition units—in all cases for parallel ports, and in several cases, for the IEEE-488 bus as well.

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Stamford, CT
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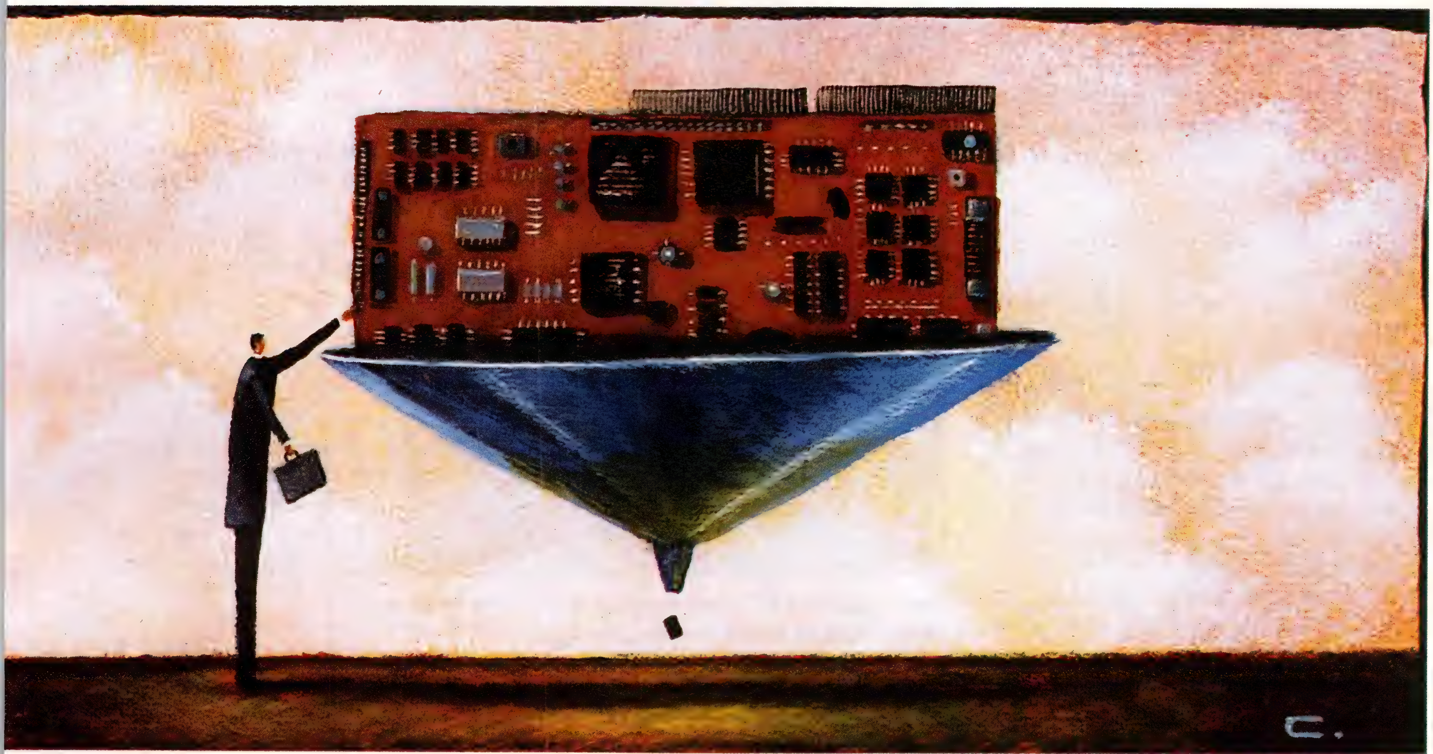

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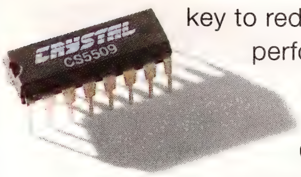

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bit, 100k-sample/sec ADCs begin at about $700. Although PCMCIA cards that offer similar performance are smaller and less expensive, external units can appear attractive when you consider their expansion capabilities and the cost and size of the signal-conditioning and -termination panels you often need with the cards.

Several vendors, such as IOtech, have developed instrument-sized data-acquisition units that connect to the IEEE-488 bus. PCMCIA IEEE-488 interfaces now let you attach such units to notebook PCs. A PCMCIA IEEE-488 interface adds roughly $200 to such a data-acquisition unit's cost. Despite that cost, you may prefer IEEE-488 if, in addition to doing data acquisition, you are also controlling one or more instruments. Today, most test-application-development packages let you treat IEEE-488 instruments just like other data-acquisition hardware. However, you can still program IEEE-488 devices with ASCII strings. People devoted to that approach may prefer IEEE-488.

This industrial PC from Keithley Metrabyte withstands hostile environments. Though larger, heavier, and more costly than typical notebooks, it includes many features lacking in a standard notebook—for example, the ability to mount ISA bus data-acquisition cards inside and to run them at full speed.

ISA—still the standard

The ISA bus appears in the **table** mainly for reference; ISA is the standard for desktop-PC data-acquisition boards. Standard notebook PCs don't accept ISA bus boards, but external attachments (from Keithley Metrabyte, among others) let notebooks use such boards. The speed of the port that connects to the external unit determines how fast the cards can run. Keithley's DacPacs connect to the high-speed ports that several popular notebooks normally use to attach to desktop docking stations. This arrangement lets the cards run at full speed. A unit that costs $1199 holds two two-thirds-length boards; a unit that costs $1499 holds two full-size boards. Both units include NiCd batteries.

Keithley Metrabyte also sells ruggedized FieldPCs that accept ISA bus boards internally and run them at full speed. These PCs resemble notebooks, but are both larger and heavier. Still, you may find these computers (from $9869) more convenient to carry than notebooks with separate data-acquisition units.

Because PCMCIA data-acquisition cards operate from notebook PCs' battery power supplies, the cards simplify data acquisition where no ac power source is handy. Vendors of PCMCIA data-acquisition cards sometimes heavily promote a card's low power consumption. When acquiring data, some analog-input cards draw almost five times as much power as others do. (In standby mode, all cards draw reduced power, but even standby power drain varies.)

The differences among cards' power drains aren't as significant as they might seem, however. The highest power cards draw less than 0.5W. A typical notebook draws about 10W. Hence, a battery charge lasts almost as long with a high-power card as with a low-power one. But, when you evaluate notebook PCs, make sure that power dissipated within the PC does not excessively warm the PCMCIA slots. High temperatures can cause leakage and drift that degrade data-acquisition cards' performance.

Unlike PCMCIA cards, not all external data-acquisition units run from batteries. Of those that do, some use separate battery packs that increase the number of items and the weight you must carry.

External units offer considerably more flexibility than do PCMCIA data-acquisition cards, however. External units often run faster and accommodate more channels, and many units provide DAC outputs in addition to

(continued on pg 61)

LOOKING AHEAD

Like so many other parts of electronics, PC-based data acquisition has changed for the better and forever because of miniaturization. The demand will only accelerate for portable data-acquisition hardware that is more capable, rugged, and cost-effective. Although PCMCIA data-acquisition cards will form a significant part of the market, such cards won't supplant more conventionally packaged hardware in the near future.

Even when PCMCIA's "teething" problems are only unpleasant memories, many users will demand more ruggedness than the diminutive cards can supply. For these users, a growing list of companies will provide small, light, high-performance equipment in somewhat larger packages. Some of these units will perform functions unlikely to appear on PCMCIA cards for several years. A product that seems to offer a glimpse of such things is IOtech's $2495, eight-channel Wavebook/512, a DSP-based, external unit that takes 1M samples/sec. Meanwhile, PCMCIA cards' performance will continue to improve, so that users who can take advantage of the cards' size will have a growing array of options.

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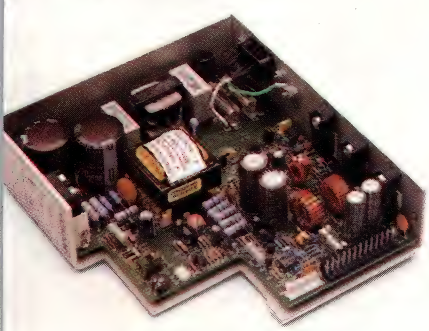

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CIRCLE NO. 144

analog inputs and digital I/O points. (The DAC outputs, a standard feature of ISA bus analog-input boards, are uncommon on PCMCIA versions.) Often, too, external units' counter/timer and triggering facilities are more flexible than those of PCMCIA cards.

Many external units also accept signal-conditioning circuits that convert the low-level outputs of popular transducers to the high levels that most data-acquisition cards' analog inputs need. In some cases, the signal-conditioning circuits also provide transducer excitation and input-to-output ohmic isolation.

Some external units incorporate signal-termination blocks. Most users of data-acquisition equipment find soldering or crimping of connectors onto transducer wiring (field wiring) impractical. These users prefer screw-terminal blocks or other connection hardware that accepts individual wires. With some of these wiring devices, you don't even need to use a screwdriver.

PCMCIA cards are much too tiny and thin to accept field wiring directly. All vendors offer separate signal-termination units (STUs) for field wiring. A prewired cable runs from the STU to a miniature connector that forms the outer edge of the PCMCIA card. STUs vary considerably in size and in the range of wire sizes they accept. Some vendors include the price of one STU in the price of a card, but you are likely to want extra STUs, which cost from under \$50 to over \$200 each. Differences among STUs justify this wide price range.

STUs can be handy if the transducers' signals are directly compatible with the data-acquisition system's inputs. You may want to wire several STUs to different parts of your test setup and take advantage of the data-acquisition system's portability. You can carry a notebook PC around the setup and plug each of the STU cables in turn onto the PCMCIA data-acquisition card, gathering a few seconds or a few minutes of data at each stop.

When signals require conditioning to make them compatible with data-acquisition-system inputs, a PCMCIA data-acquisition card's advantages over an external data-acquisition unit are less clear. One way to use a PCMCIA ADC card in such situations is to deploy manifolds of signal conditioners around the test setup in place of STUs. The manifolds of signal conditioners cost much more than STUs, however, so this approach isn't necessarily economical.

Alternatively, you can move a manifold of signal conditioners around with the notebook PC. To connect the transducers to the manifold, you probably should use an STU that you can plug into the manifold. Such an arrangement avoids the need to shut down the experiment to connect the data-acquisition system. However, when you carry around a setup that includes a signal-conditioner manifold, you're transporting a system that's about as large and heavy as one based on an external data-acquisition unit. Moreover, if both systems use plug-in STUs, the systems are equally easy to connect.

Compared with personal computing, and especially with notebook PCs, the pace of change in data acquisition—at least on the hardware side—appears glacial. But the marriage of portable computing and data acquisition has permanently changed data acquisition. PCMCIA data-acquisition cards are a stunning development. External units for notebook PCs, though lacking in some of the tiny cards' futuristic flavor, can be equally useful. When all questions require answers yesterday, portable data-acquisition equipment often offers the only hope of getting the necessary information on time. EDN

You can reach Senior Technical Editor Dan Strassberg at (617) 558-4205, fax (617) 928-4205, e-mail: ednstrassberg@cahners.com

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Video fader preserves synchronization

FRANK COX, LINEAR TECHNOLOGY CORP, MILPITAS, CA

The common video effect "fade to black" is usually accomplished by increasing video signal attenuation to the point where the picture disappears, leaving a black screen. As the composite signal is attenuated, the signal's sync amplitude becomes too small to synchronize the picture properly, and the picture rolls and tears. One solution is to run a separate sync line to the monitor, but this is not a viable choice in composite systems.

Fig 1 shows a simple video "volume control" that operates on the picture but leaves the sync unchanged, allowing a smooth fade to black while maintaining video fidelity. High-speed op-amp IC_1 and its associated components form a basic sync separator. C_1, R_1, and D_1 clamp and clip composite video. D_2 biases the input of IC_1 to compensate for the voltage drop across D_1. When D_1 conducts, IC_1 amplifies the most negative portion of the waveform (containing the sync information). Clamp-network D_4 through D_7 in the feedback of IC_1 prevents the amplifier from saturating and, thus, from slowing the response. D_3 and a CMOS inverter complete the shaping of the sync waveform. The sync separator works with most video signals that have a minimum sync amplitude of 0.3V and are not excessively noisy or distorted.

Video-fader IC_2 is configured to fade between the original video and the sync stripped from that video. A voltage reference and a potentiometer generate a control voltage. This node (pin 3 of IC_2) should be bypassed if the control is mounted a significant distance from the circuit or if the control generates any noise when adjusted. As the control voltage nears the lower 2% of its range, IC_2 automatically shuts off the channel with the active video (pin 1) and fully turns on the channel with the sync (pin 14). This feature makes the circuit more tolerant of offset or gain errors in the control signal. (DI #1724)

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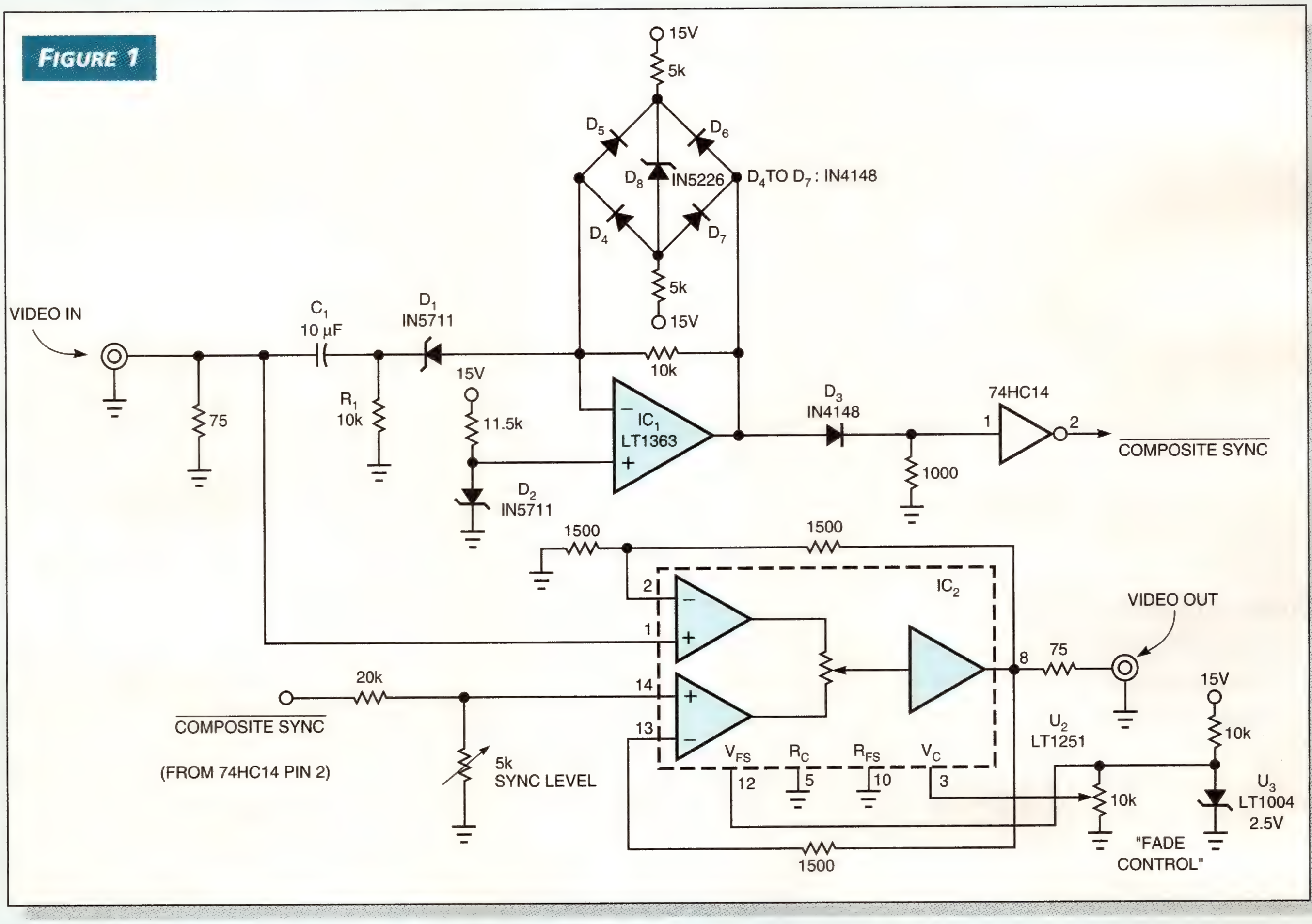
FIGURE 1



This circuit allows you to maintain sync amplitude while fading a composite-video signal.

Behavioral Spice model emulates VCO

DR BASHIR AL-HASHIMI, STAFFORDSHIRE UNIVERSITY, STAFFORD, UK

A behavioral model treats a circuit as a black box, which you can describe using an equation or table. **Listing 1** is a Microsim PSpice behavioral model that simulates the operation of a voltage-controlled oscillator (VCO). The output signal of a VCO is $V_O=A\cdot\sin(2\pi f_O t)$, where A is the amplitude, t is the time variable, and f_O is the output frequency. This frequency is $f_O=f_C+KV$, where f_C is the center frequency, K is the sensitivity of the VCO in Hz/V, and V is the control-input signal.

The model expresses these equations using a VALUE description of a voltage-controlled voltage source. Note that the parameter TIME in the model represents the PSpice internal sweep variable used in transient analysis. To simplify use of the model, describe it as a parameterized subcircuit called VCO, whose input is at node 1 and whose output is at node 2. Describe the model function using the three parameters A, f_C, and K. You must give the subcircuit parameters initial values to satisfy the .SUBCKT statement requirement. In this example, I arbitrarily set them to one; you'll change them to the required values when the program calls the subcircuit.

To use the model to simulate a VCO circuit, specify the parameters A, f_C, and K. For example, if A=2V, f_C=10 kHz, K=5 kHz/V, and the input control voltage ranges from +1 to –1V, the output frequency changes from 15 to 5 kHz, as **Fig 1** shows. **Listing 2** gives the PSpice netlist of the VCO circuit. (DI #1726)

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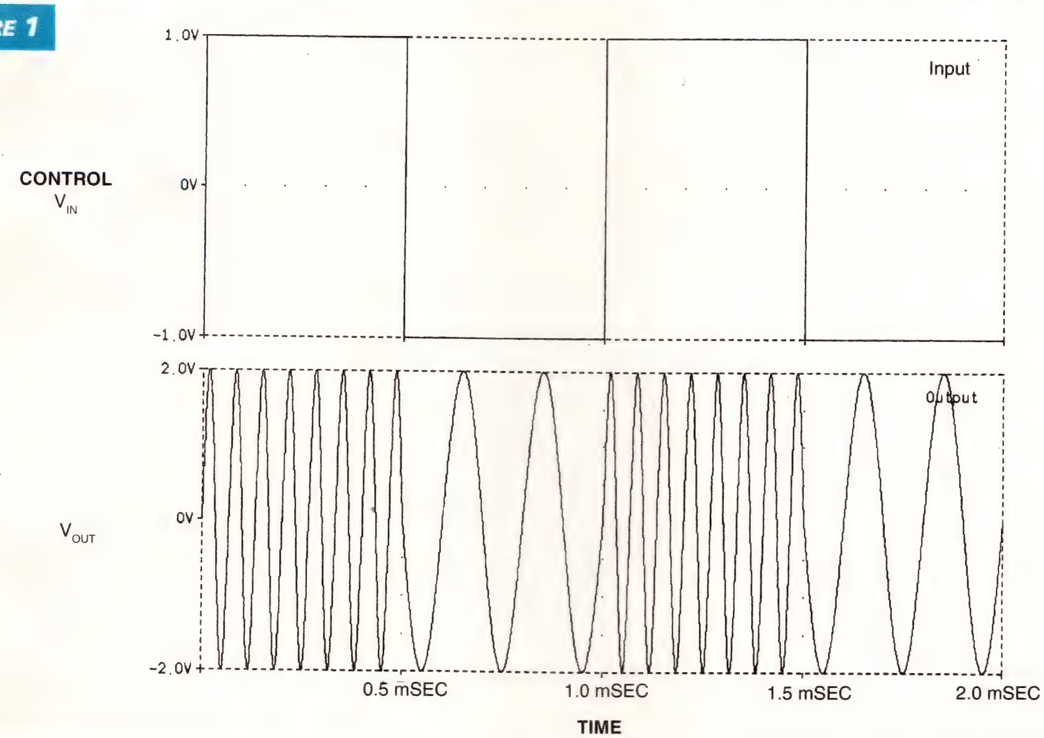
LISTING 1—VCO BEHAVIORAL MODEL

```
.SUBCKT VCO 1 2 PARAMS:A=1, Fc=1, K=1
E 2 0 VALUE={A*SIN(6.283*TIME*(Fc+K*V(1,0)))
.ENDS VCO
```

LISTING 2—VCO-CIRCUIT PSPICE NETLIST

```
.LIB C:\PSPICE\MODELS ;VCO model location
V 1 0 PULSE(-1 1 0 10ns 10ns 0.5ms 1ms) ;control input signal
.TRAN 0.01m 2ms 0m 0.01m ;transient analysis range
X 1 2 VCO PARAMS:A=1, Fc=10K,K=5K ;call VCO subcircuit
.PROBE V(1),V(2) ;graphic input & output signals
.END ;end of netlist
```

FIGURE 1



The bottom plot shows the result of a PSpice simulation of a VCO. When the control-input voltage changes from +1 to –1V, the output frequency changes from 15 to 5 kHz.

Circuit guards against battery reversal

DANA DAVIS, MAXIM INTEGRATED PRODUCTS, SUNNYVALE, CA

The circuit in **Fig 1** protects a battery-operated system in two ways: Q_1 prevents damage from the flow of reverse current that could occur if you install the battery backward, and Q_3 prevents the excessive current flow that could occur with a sudden load increase or a short circuit. A properly installed battery fully enhances Q_1 by pulling its gate voltage more than 5V below the source voltage. If you install the battery backward, Q_1 stays off because the gate voltage is positive with respect to the source voltage. Regardless of battery polarity, the orientation of the body diodes of Q_1 and Q_3 ensures that no current can flow when either device is off.

IC_2 is a current-sensing amplifier that senses the load current flowing between its RS+ and RS– terminals. IC_2's output is a proportional but smaller (1.5 mA max) current at the OUT pin, which develops a voltage across R_8 proportional to the load current. During normal operation, both comparator outputs are high, and Q_3 remains on.

When the load current exceeds a limit set by R_8 (I_{LIMIT}= $2000V_{TH}/R_8$), where 2000 is the sense amplifier's gain, and V_{TH} is the comparator's input threshold of 1.182V ±2%, the B-comparator output switches low and turns off Q_4, which turns off Q_3 and disconnects the battery from its load. At the same time, Q_6 provides positive feedback by pulling the comparator input to the level of the collapsing supply rail, latching Q_3 off as the supply voltage drops.

An output short turns off IC_2 by removing the voltage at pins 6 and 7 (3V is the minimum for proper operation). Control via the B comparator disappears because the R_8 voltage goes to zero for this short-circuit condition, but comparator A then shuts off Q_3 by turning off Q_5. Q_2 speeds the Q_3 turn-off time to about 10 μsec. When Q_3 is off, the circuit draws about 2 μA. During normal operation, the battery current varies with its terminal voltage: 200 μA at 5V, 230 μA at 6V, 300 μA at 8V, and 310 μA at 10V. To restore power, press S_1. (DI #1730)

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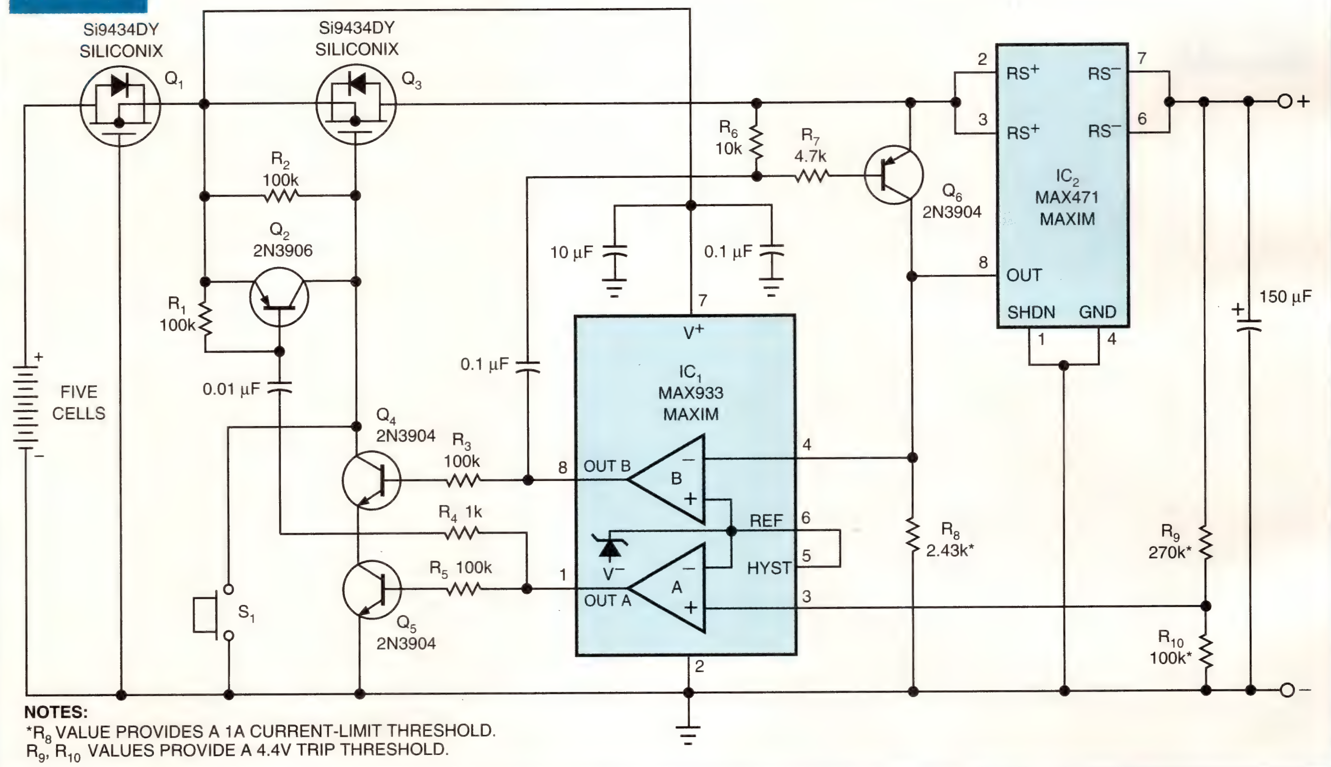
FIGURE 1



This circuit prevents damage from reverse current that flows when a battery is installed backward. The circuit also prevents excessive current flow that arises from a sudden load step or short circuit.

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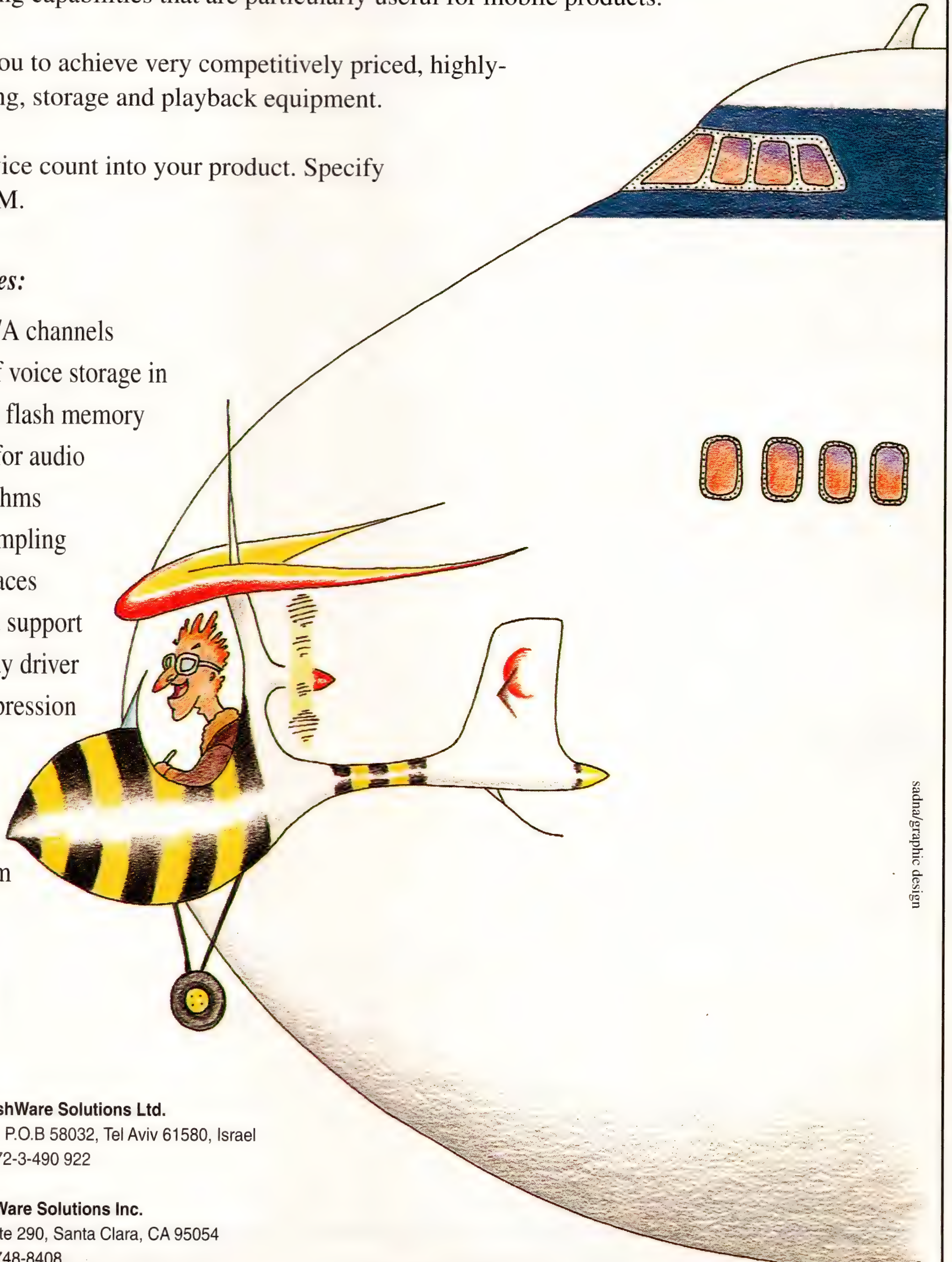

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CIRCLE NO. 228

Measure inductance with dc superimposed

HB FARENSBACH, CONSULTANT, ALBANO, ITALY

In some applications, magnetic components are difficult to characterize when steady-state current is flowing. Bridges having the necessary dc capability are expensive. If you don't need extreme precision (for example, 2% or better), other measurement methods exist. The method in **Fig 1** is universally applicable over a range of inductances and frequencies. The basis for the inductance measurement is to determine the ac impedance at the frequency (f), ideally the inductor's working frequency of interest. In **Fig 1**, the ac voltages across the inductor and the reference resistor R_R are V_{LAC} and V_{RAC}, respectively, and the circulating alternating current is I_{AC}.

You need the following two components for proper operation: 1. The dc isolation transformer with a gap that prevents saturation at the maximum rated dc. In this example, for 25A current, use an EI-configured core of 0.014-in. grain-oriented silicon steel. The primary winding uses 160 turns of AWG 30 double-covered magnet wire. The secondary winding consists of 32 turns of AWG 14 magnet wire wound in two steps: 16 turns, followed by the primary winding, followed by the final 16 turns. 2. The reference resistor, which must have four terminals (two for forcing current, two for sensing voltage) if its value is lower than 3Ω. It also must have negligible inductance and skin effect at the frequency of interest. One way to make a resistor with such characteristics is to connect several (maybe five to 10) metal-film resistors in parallel.

To keep errors low, ensure that $3V_{RAC}$ is less than V_{LAC}. Check oscilloscope photos to be sure the waveforms are reasonably sinusoidal, denoting that the flux density is below the saturation level. You can also measure the dc I_{DC} by using the same DVM or the oscilloscope in dc mode. To determine the impedance, Z_L, use the following equations:

$$Z_L = \frac{V_{LAC}}{I_{LAC}} = \frac{V_{LAC} \times R_R}{V_{RAC}}$$

$$L = \frac{Z_L}{2\pi f} = \frac{V_{LAC} \times R_R}{2\pi f\ V_{RAC}}$$

The error in V_{LAC} from V_{RAC} is negligible because these two quantities are 90° out of phase. Measure both V_{LAC} and V_{RAC} the same way—by using the oscilloscope's p-p value, the DVM's average value, or the DVM's rms value. The power supply should have 3 to 5% maximum ripple and a constant-current setting for ease of making repeated measurements. The zener diodes across the primary winding protect the frequency generator against spikes that occur when you instantaneously apply or cut off the dc.

An example uses a 50-μH inductor operating at 100 kHz, with a 100-mΩ reference resistor, R_R. Measurements yield V_{RDC}=1V (10A), V_{LAC}=1.2V, and V_{RAC}=38 mV.

$$L = \frac{V_{LAC}R_R}{2\pi f\ V_{RAC}} = \frac{1.2V \times 0.100\Omega}{6.28 \times 100{,}000\ Hz \times 0.038V} = 5.03\ \mu H$$

(DI #1729)

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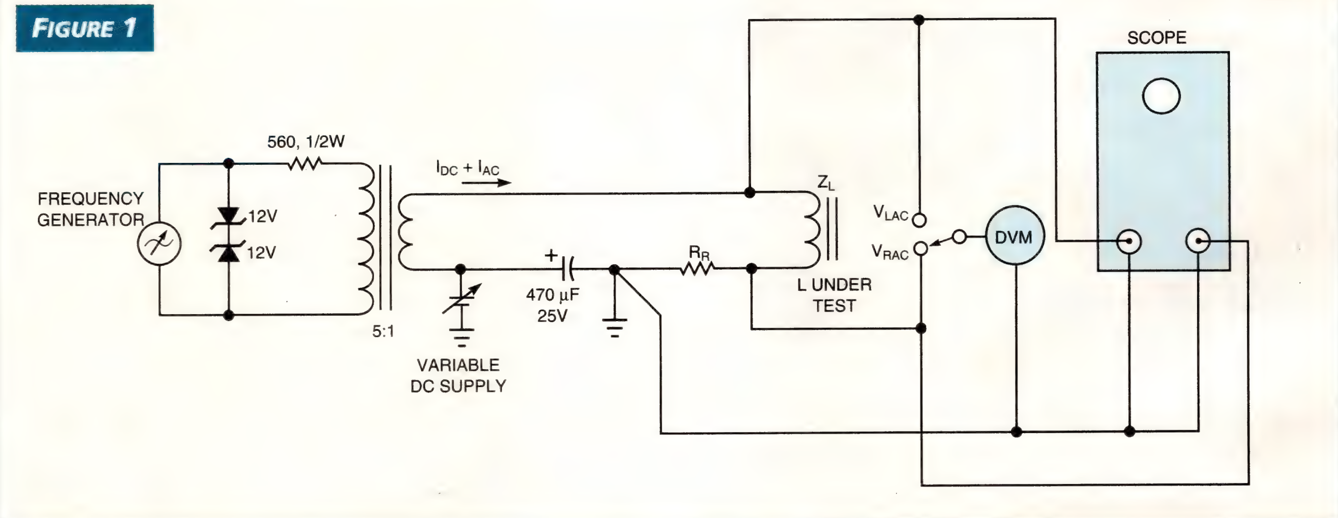
FIGURE 1



Using this circuit, you can measure inductance with any amount of direct current superimposed.

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CIRCLE NO. 188

"Zero-power" A/D converter uses printer port

DHANANJAY GADRE, IUCAA INSTRUMENTATION LAB, PUNE, INDIA

BBS

You can use a desktop or laptop PC to monitor physical variables such as temperature or pressure. A convenient way to do this is to connect an A/D converter through the ubiquitous Centronics printer port (**Fig 1**). The current requirement of the ADC0804LCN used here is less than 1.5 mA at 5V supply voltage with a 640-kHz clock. Tristate-buffer 74HC244 multiplexes 8 bits of A/D-converter data through 4 bits (54 through 57) of the status port of the printer adapter.

This design does not require an external power supply, because it uses the RS-232C port of the PC to satisfy its meager power requirements. Most RS-232C ports are capable of delivering a current of about 10 mA. Of this current budget, the circuit shown here consumes about 3 mA. You could use the remaining available current to power additional circuitry. The 5V for the A/D converter and the tristate switch derives from the RS-232C port's DTR and RTS signal lines. Because the power requirement is low, you can use a pair of LM-336-2.5V reference diodes to set the voltage and to generate the 2.5V reference for the A/D converter.

Control-port bits C0 and C1 control the tristate switch, IC_2. The power-on reset level of C0 and C1 is logic one, so you run no risk of shorting IC_2's outputs. The other 2 control bits, C2 and C3, generate the read and write strobes for the A/D converter. The INTR pin of the A/D converter, which status-port bit S3 monitors, indicates end of conversion for the converter. With the component values shown, the converter has a 200-μsec conversion time on a 16-MHz AT, running the C code in **Listing 1**. A Turbo C version 2.01 compiler compiled this source code. (DI #1728) EDN

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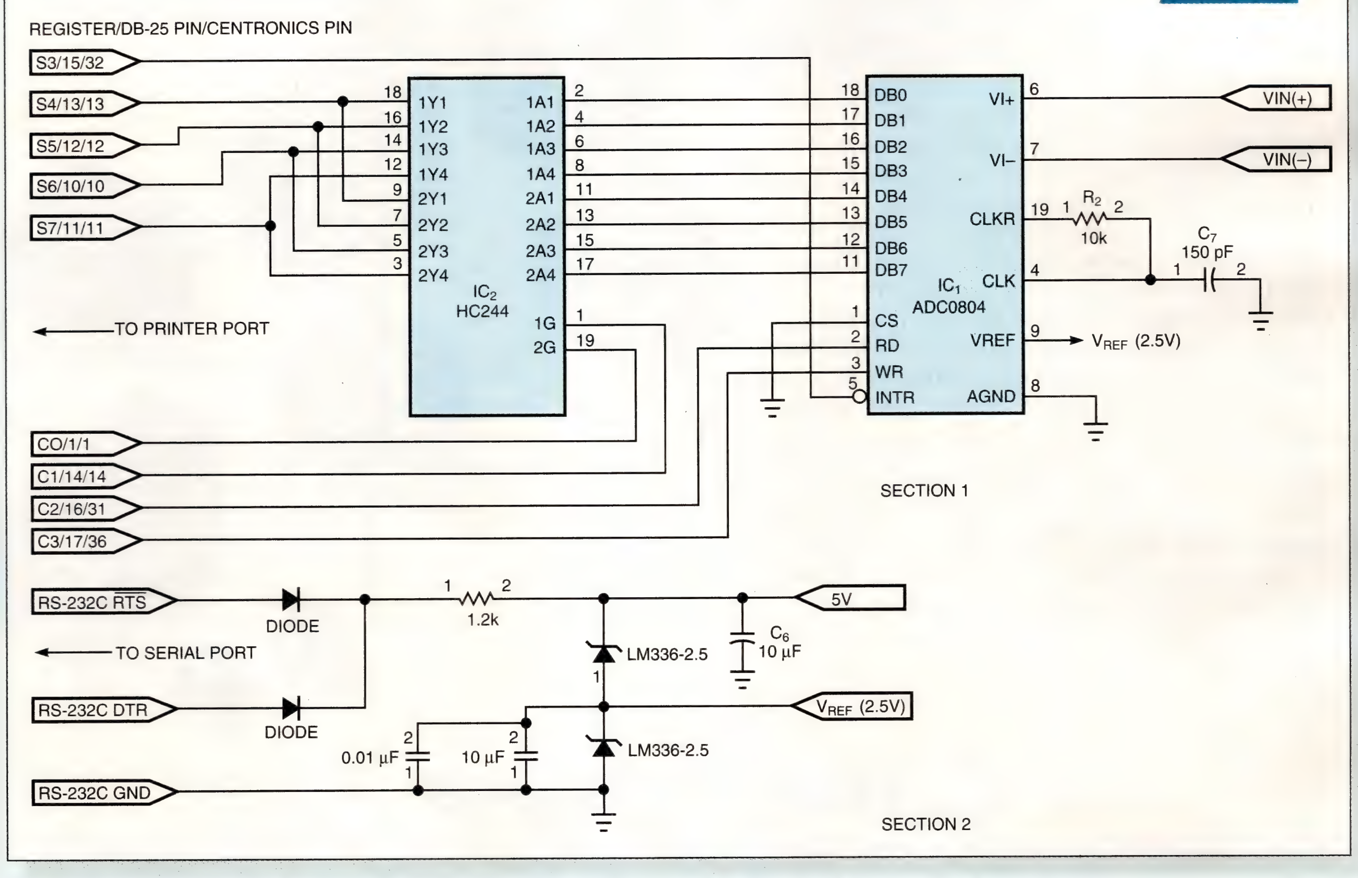
(Listing 1 on pg 72)

FIGURE 1



This A/D converter takes its power from the PC's RS-232C port and thus needs no external power source.

LISTING 1—SOURCE CODE FOR ZERO-POWER A/D CONVERTER

```
#include  <stdio.h>
#include  <dos.h>
#include  <conio.h>
#include  <process.h>
                                                  /*  C3* C2  C1* C0*  */
#define RESET_VALUE         0X04                  /*  0   1   0   0    */
#define START_ADC_CONV      0X0c                  /*  1   1   0   0    */
#define READ_UPPER_NIBBLE   0X01                  /*  0   0   0   1    */
#define READ_LOWER_NIBBLE   0X02                  /*  0   0   1   0    */

void main(void)
{
int modem_control_reg, dport_lpt1, cport_lpt1, sport_lpt1;
unsigned char adc_status, adc_val, upper_nib, lower_nib, intr_status;

/* Sign ON */
clrscr();
printf("Zero power (well almost) ADC for printer port, Version 1.0");
printf("\nD.V.GADRE");

/* Get COM1 register address */
modem_control_reg = peek(0x40,0)+4;
if(modem_control_reg == 4)
          (printf("\n\n\nCOM1 not available... aborting\n\n\n");
          exit(1);
          }
printf("\n\n\nCOM1 address = %X",peek(0x40,0) );

/*Get LPT1 port addresses */
dport_lpt1 = peek(0x40,0x08);
if(dport_lpt1 ==0)
          {
          printf("\n\n\nLPT1 not available... aborting\n\n\n");
          exit(1);
          }
printf("\nLPT1 address = %X", dport_lpt1);
cport_lpt1 = dport_lpt1 +2;      /* control port address */
sport_lpt1 = dport_lpt1 +1;      /* status port address  */

/* put power  On  on  COM1  */
outportb(modem_control_reg, 03);
printf("\nPutting Power ON...");

/* check if ADC is connected & working */
/* start ADC conversion & wait for 1 ms, this puts INTR to logic '0' */
/* reset the control port */
outportb(cport_lpt1, RESET_VALUE);
sleep(1);

/* start conversion */
outportb(cport_lpt1, START_ADC_ CONV);
outportb(cport_lpt1, RESET_VALUE );
sleep(1);

/* hopefully the conversion is over, so read the INTR status */
/* if everything is OK, INTR should be '0' */
adc_status = inportb(sport_lpt1) & 0x08;
outportb(cport_lpt1, READ_LOWER_NIBBLE);
outportb(cport_lpt1, RESET_VALUE);

/* read the INTR status again */
/* if everything is OK, INTR should be '1' */
intr_status = inportb(sport_lpt1) & 0x08;
if( !( (adc_status == 0) && (intr_status == 0x08) ) )
        { printf("\n\n\nADC not connected... aborting\n\n\n");
          exit(1);
         }

/* acquire ADC sample */
while(!kbhit())
                {
                        outportb(cport_lpt1, RESET_VALUE);
start_conv:             outportb(cport_lpt1, START_ADC_CONV);
                        outportb(cport_lpt1, RESET_VALUE);
wait_for_conv:          adc_status = inportb(sport_lpt1) & 0x08;
                        while(adc_status)
                        {
                        adc_status = inportb(sport_lpt1) & 0x08;
                        }
read_upper_nibble:      outportb(cport_lpt1, READ_UPPER_NIBBLE);
                        upper_nib = inportb(sport_lpt1) & 0x0f0;
                        outportb(cport_lpt1, RESET_VALUE);
read_lower_nibble:      outportb(cport_lpt1, READ_LOWER_NIBBLE);
                        lower_nib = inportb(sport_lpt1) >> 4;
                        outportb(cport_lpt1, RESET_VALUE);
     adc_val = (lower_nib | upper_nib) ^ 0x88;
     delay(10);
     printf("sample = %X ", adc_val);
```

Serial-interface IC supplies bipolar voltages

GARY SELLANI, MAXIM INTEGRATED PRODUCTS, SUNNYVALE, CA

Some available ICs for serial-data interface not only operate from low supply-rail voltages (5 or 3.3V) but also generate bipolar dc voltages (±6.5 to ±10V) to meet minimum driver-output levels specified by EIA/TIA-232. With care, you can "steal" useful amounts of power from these rails without interfering with the IC's operation.

In **Fig 1**, switch-mode-controller IC_1 operates with an external inductor, two diodes, and two capacitors to produce ±6.5V. FETs Q_1 and Q_2 ensure start-up for the circuit by disconnecting the load until these switch-mode supply voltages are present. Q_1 must be a logic-level device.

Unlike ICs designed to generate supply voltages, an interface IC generally doesn't specify how much current you can draw from its internally generated supply rails. The amount available depends almost entirely on loads connected to the driver outputs. For example, IC_1 guarantees that one transmitter can drive a parallel combination of 1 kΩ and 1000 pF at 250 kbps, and the other two transmitters can maintain dc outputs across 3-kΩ loads.

To calculate the maximum output current available, superimpose the ac and dc components. Output current flows alternately from each rail as the NRZ output waveform swings between the guaranteed-minimum-output levels (±5V). Assuming the output requires one whole data period (4 μsec at 250 kbps) to slew from –5 to +5V, the ac component equals C_{LOAD}(dV/dt)=1000 pF (10V/4 μsec)=2.5 mA. For the dc component, Ohm's law gives I=E/R=5V/3 kΩ=1.67 mA from one transmitter, so the three transmitters together

represent a dc load of 5 mA. Adding the ac and dc components gives a conservative maximum rating of 2.5 mA+5 mA=7.5 mA.

The 3-kΩ load is an EIA-232 requirement, but the data rate and load capacitance are application-dependent parameters. Lower values for these parameters make more current available for external use. A remote-sensing system, for instance, might operate at 2400 bps with a load of 3 kΩ in parallel with 1000 pF (50 ft of cable at 20 pF/ft). For three transmitters, the load is 5 mA, and the ac load for one transmitter (72 μA) is almost negligible in this low-data-rate application. The available current in this case is calculated as 7.5 mA–(5 mA+72 μA)=2.428 mA.

These calculations are conservative: With V_{CC} at 2.7V and the three transmitters loaded with 3 kΩ/1000 pF while transmitting valid EIA-232 levels at 2400 bps, the circuit actually delivers 6.7 mA to an external load. As noted, Q_1 and Q_2 allow the circuit to start under these conditions. If you disconnect the transmitter loads, the maximum external load current that allows start-up is 11.5 mA; with Q_1 and Q_2 removed, the maximum current is only 5.7 mA. (DI #1725)

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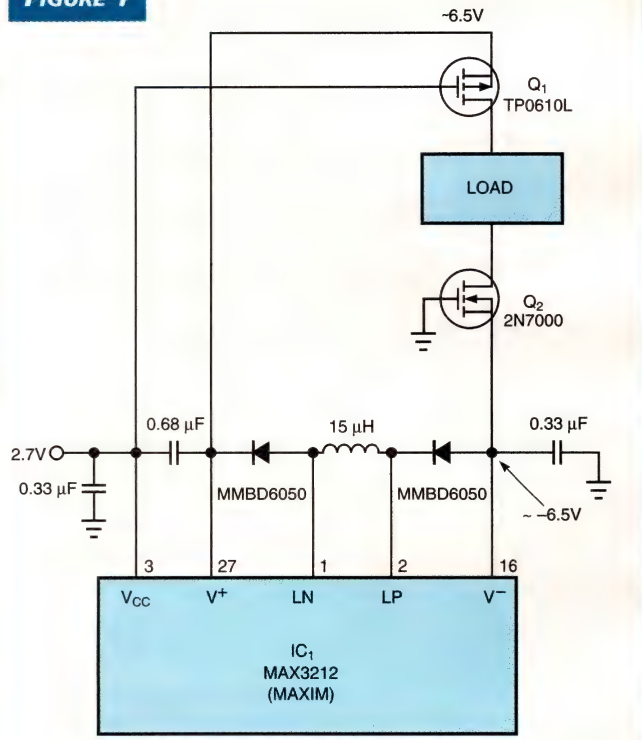
FIGURE 1



For data rates and driver-output loads less than the maximum allowed, the positive and negative voltage outputs of this serial-interface IC can supply modest amounts of current to an external circuit.

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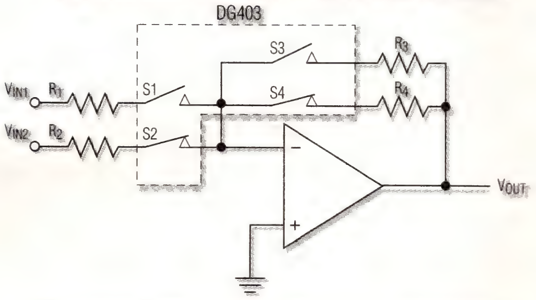

Switching into a virtual ground reduces distortion caused by $R_{DS(ON)}$ variation over the analog signal range. Guaranteed $R_{DS(ON)}$ matching (typically 0.5Ω) ensures gain accuracy of <0.01% when R1 through R4 are greater than 10kΩ.

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DG411/2/3	3	4	10	5	10
DG417/8/9	3	4	10	5	10
DG421/3/5	3	4	15	5	10
DG441/2/4/5	3	9	10	5	10

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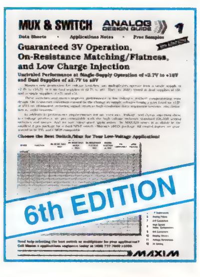

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LINEAR TECHNOLOGY DESIGN NOTES

C-Load™ Op Amps Conquer Instabilities – Design Note 107

Kevin R. Hoskins

Introduction

Linear Technology Corporation has taken advantage of advances in process technology and circuit innovations to create a series of C-Load operational amplifiers that are tolerant of capacitive loading, including the ultimate, amplifiers that remain stable driving any capacitive load. This series of amplifiers have a bandwidth that ranges from 160kHz to 140MHz. These amplifiers are appropriate for a wide range of applications from coaxial cable drivers to analog-to-digital converter (ADC) input buffer/amplifiers.

Driving ADCs

Most contemporary ADCs incorporate a sample-and-hold (S/H). A typical S/H circuit is shown in Figure 1. The hold capacitor's (C1) size varies with the ADC's resolution but is generally in the range of 5pF to 20pF, 10pF to 30pF and 10pF to 50pF for 8-, 10- and 12-bit ADCs, respectively.

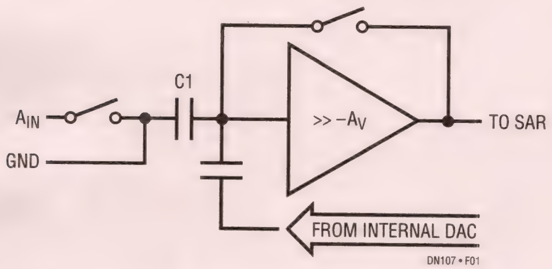

Figure 1. Typical ADC Input Stage Showing Input Capacitors

At the beginning of a conversion cycle, this circuit samples the applied signal's voltage magnitude and stores it on its hold capacitor. Each time the switch opens or closes, the amplifier driving the S/H's input faces a dynamically changing capacitive load. This condition generates current spikes on the input signal. This capacitive load and the spikes produced when they are switched constitutes a very challenging load that can potentially produce instabilities in an amplifier driving the ADC's input. These instabilities make it difficult for an amplifier to quickly settle. If the output of an amplifier has not settled to a value that falls within the error band of the ADC, conversion errors will result. That is unless the amplifier is designed to gracefully and accurately drive capacitive loads, such as Linear Technology's C-Load line of monolithic amplifiers. Table 1 lists Linear Technology's unconditionally stable voltage feedback C-Load amplifiers. Table 2 lists other voltage feedback C-Load amplifiers that are stable with loads up to 10,000pF.

Table 1. Unity-Gain Stable C-Load Amplifiers Stable with All Capacitive Loads

SINGLES	DUALS	QUADS	GBW (MHz)	I_S/AMP (mA)
—	LT®1368	LT1369	0.16	0.375
LT1200	LT1201	LT1202	11	1
LT1220	—	—	45	8
LT1224	LT1208	LT1209	45	7
LT1354	LT1355	LT1356	12	1
LT1357	LT1358	LT1359	25	2
LT1360	LT1361	LT1362	50	4
LT1363	LT1364	LT1365	70	6

Table 2. Unity-Gain Stable C-Load Amplifiers Stable with $C_L \leq$ 10,000pF

SINGLES	DUALS	QUADS	GBW (MHz)	I_S/AMP (mA)
LT1012	—	—	0.6	0.4
—	LT1112	LT1114	0.65	0.32
LT1097	—	—	0.7	0.35
—	LT1457	—	2	1.6

Remaining Stable in the Face of Difficult Loads

As can be seen in Figure 2, an amplifier whose design is not optimized for handling a large capacitive load, has some trouble driving the hold capacitor of the LTC®1410's S/H. While the LT1006 has other very desirable characteristics such as very low V_{OS}, very low offset drift, and low

power dissipation, it has difficulty accurately responding to dynamically changing capacitive loads and the current glitches and transients they produce (as indicated by the instabilities that appear in the lower trace of Figure 2a.

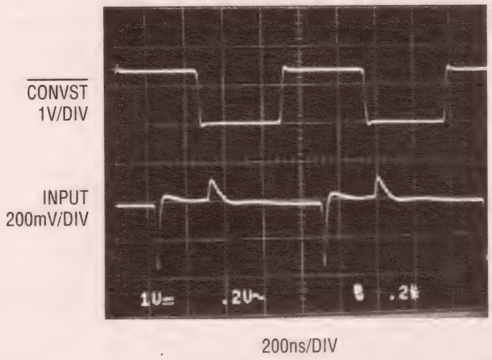

Figure 2a. Input Signal Applied to an LTC1410 Driven by an LT1006

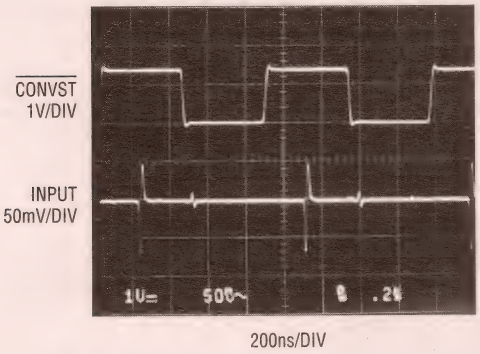

Figure 2b. Input Signal Applied to an LTC1410 Driven by an LT1360

By contrast, Figure 2b shows the LTC1360 C-Load op amp driving the same LTC1410 input. The photo shows that the LTC1360 is an ideal solution for driving the ADC's input capacitor quickly and cleanly with excellent stability. Its wide 50MHz gain-bandwidth and 800V/μs slew rate very adequately complement the LTC1410's 20MHz full power bandwidth. The LTC1360 is specified for ±5V operation.

Figure 3 shows the circuit used to test the performance of op amps driving the LTC1410's input and measure the input waveforms.

Conclusion

Linear Technology's C-Load amplifiers meet the challenging and difficult capacitive loads of contemporary ADC analog inputs by remaining stable and settling quickly.

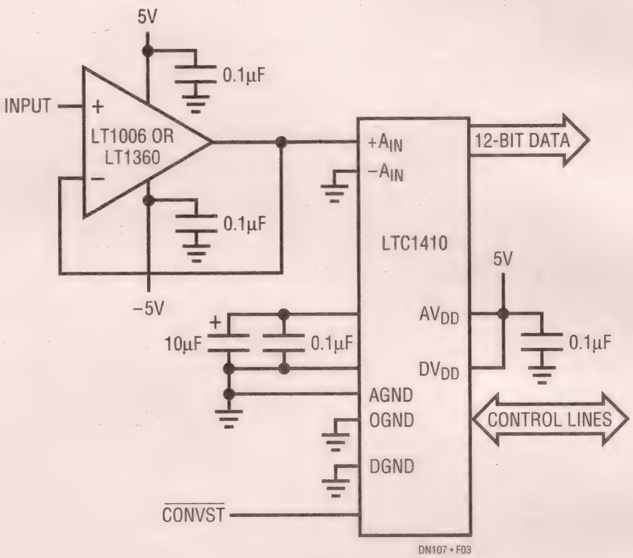

Figure 3. Test Circuit Used to Measure LTC1410 Input Signal Waveform

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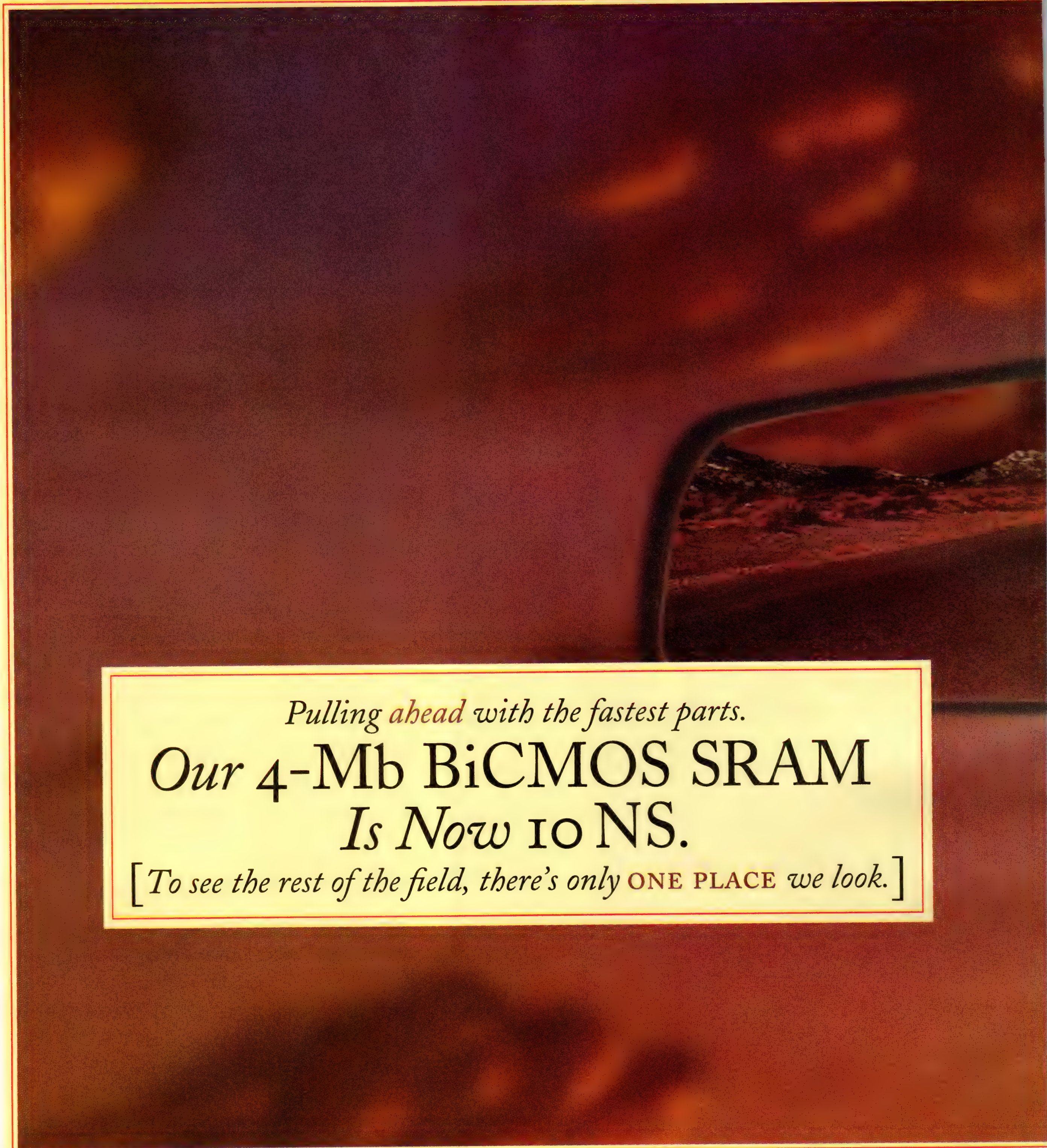

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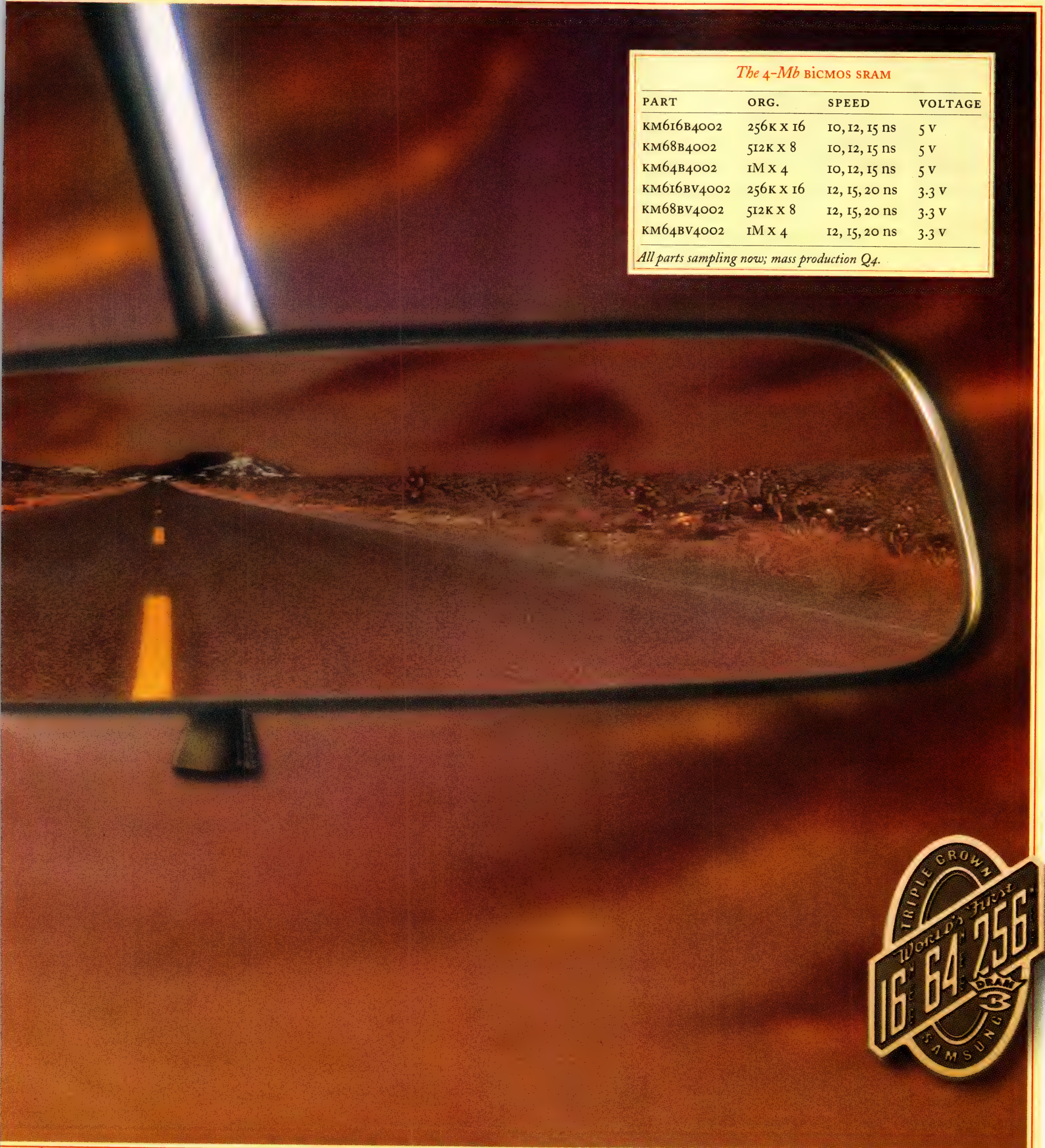

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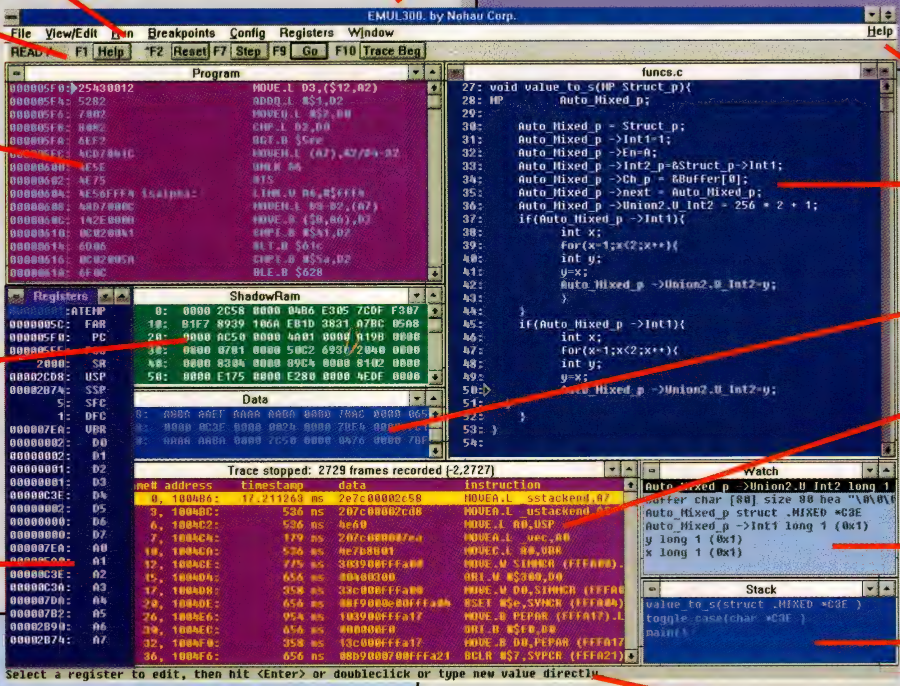

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CIRCLE NO. 213

Optimize sensor systems using fixed components

ERIC JACOBSEN AND JEFF BAUM, MOTOROLA SENSOR PRODUCTS DIVISION

A design method that uses device-to-device variations, temperature effects, and component tolerances allows you to configure optimum amplifier and ADC circuitry for sensor systems.

A circuit design for a sensor system with fixed-value components is easier and less costly to produce in high volume. The alternatives to using fixed-value circuitry—laser-trimming resistors, manually calibrating potentiometers, or measuring and selecting specific component values—are labor-intensive. Fixed-value components combine with a design procedure to optimize the performance of a sensor system using standard components. The method considers device-to-device, temperature, and other circuit variations that can create alterations in the amplified sensor output.

The method starts with a desired performance and set parameters. The design then considers each type of variation in a worst-case analysis to determine if the system can attain the desired performance. Every sensor type has device-to-device variations in the output offset voltage, the full-scale output voltage, and the dynamic output-voltage range. (Span is the difference between full-scale and zero-scale output voltage.) These parameters vary with temperature, according to the temperature coefficients (TCs) of offset, TCV_{OFF}, and full-scale span, TCV_{FSS}. The fixed-value circuit comprising the sensor has variations. For example, the voltage or current regulator and resistors have specified tolerances and TCs.

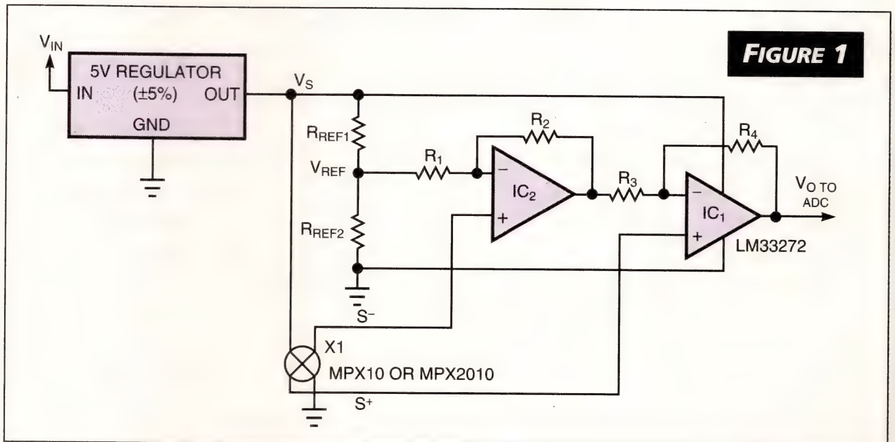
Because modern, unamplified solid-state sensors typically have output voltages of 10s of millivolts, a gain stage is a major part of the fixed-value circuitry. The gain stage amplifies the signal to a level large enough for additional processing. One such sensor, Motorola's MPX10 10-kPa pressure sensor, has a typical full-scale span of 58 mV at 5V excitation. The additional processing typically requires using an A/D converter to digitize the amplified analog sensor signal.

The ADC window is the difference between its high and low reference voltages. To obtain the best signal resolution from an ADC, the sensor's amplified dynamic output-voltage range should fill as much of the ADC's window as possible without extending beyond the reference voltages. The zero-pressure offset voltage must be greater than or equal to the low reference voltage, and the full-scale output voltage must be less than or equal to the high reference voltage. In any case, the device-to-device, temperature, and circuit variations create a problem.

With a fixed-value amplifier circuit, the gain and any dc level shift inherent in the amplifier design are fixed. If the variation of any sensor parameters is too large, the amplified sensor output may saturate the amplifier near either its high or its low supply rail. The output may also extend beyond the high or low reference voltages of the ADC. In either case, nonlinearity errors occur in the system. To avoid such errors, you should design a fixed-value circuit that optimizes performance in terms of signal resolution and takes all types of sensor-output variation into account.

The goal of the fixed-value sensor system is to obtain the best performance possible. The system's design needs to ensure that the sensor's amplified output is always within the saturation levels of the amplifier and reference levels of

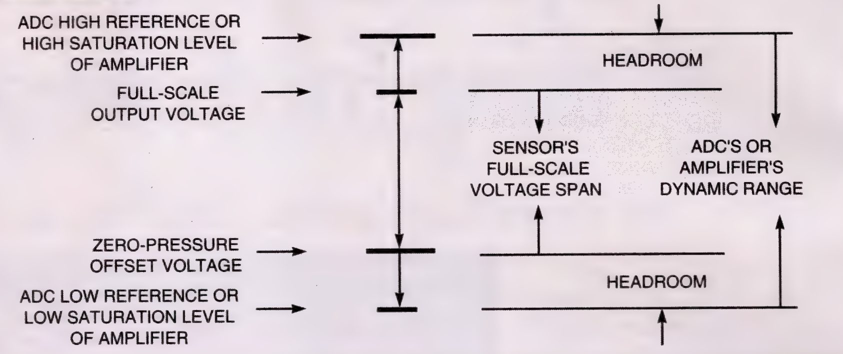
FIGURE 1



This amplifier circuit scales up the low-level output voltage of an IC pressure sensor for processing by an ADC.

the ADC, regardless of any system variation. Satisfying these tenets makes effecting an accurate software calibration of the sensor's output possible. By sampling the sensor's output voltage at a few points (such as, zero and full-scale output) at room temperature, a software calibration can nullify all the room-temperature, device-to-device, and circuit variations. Temperature variations in the sensor's output can create errors in the system, but careful design can ensure that the output remains within the ADC's valid range.

FIGURE 2



The difference between the offset and full-scale span of the sensor and the dynamic range of the amplifier or ADC is headroom.

Applying the method

Fig 1 shows how you can apply the method using Motorola's MPX10 and MPX2010 pressure sensors. Both sensors have a full-scale rated pressure of 10 kPa. The MPX2010 also has on-chip circuitry for calibration and temperature compensation of the zero-pressure offset voltage and span. Comparing these devices emphasizes how dramatically device-to-device and temperature variations, if not compensated, can affect a system's overall performance.

Both pressure sensors interface to the same amplifier-circuit topology. **Tables 1** and **2** give the device-to-device and temperature variations for the MPX10 and MPX2010, respectively. Additional factors to consider in the method are the voltage-regulator and resistor tolerances. The voltage regulator's device-to-device tolerance is ±5%, and each resistor's tolerance is ±1%.

TABLE 1—MPX10 PRESSURE-SENSOR VARIATION CHARACTERISTICS

Characteristic (V_S=5V)	Symbol	Minimum	Typical	Maximum	Unit
Pressure range	P_{OP}	0		10	kPa
Full-scale span	V_{FSS}	33	58	83	mV
Zero-pressure offset	V_{OFF}	0	33	58	mV
TC of full-scale span (Note 1)	TCV_{FSS}	–0.22	–0.19	–0.16	%/°C
TC of zero-pressure offset (Note 2)	TCV_{OFF}		±15		µV/°C

Notes:
1. Slope of endpoint straight line fits to full-scale span at –40 and 125°C, relative to 25°C.
2. Slope of endpoint straight line fits to zero-pressure offset at –40 and 125°C, relative to 25°C.

The amplifier topology in **Fig 1** is a two-stage operational-amplifier gain block that has the desirable characteristics of a differential-input instrumentation amplifier:

- High input impedance,
- Low output impedance,
- Differential-to-single-ended signal conversion,
- High gain, and
- Level-shifting capability.

For good common-mode rejection, the ratio of R_4 to R_3 should equal the ratio of R_1 to R_2. With this simplification, the transfer function of the amplifier is

$$V_O = \left(\frac{R_4}{R_3}+1\right)\left(S^+ - S^-\right) + V_{REF},$$

where the gain is R_4/R_3+1, and the pressure sensor's differential output voltage is $S^+–S^-$. The positive dc voltage-level shift, which the voltage divider comprising R_{REF1} and R_{REF2} creates, is V_{REF}. You should use the cited resistor-ratio equality to preserve the common-mode rejection. Also, make sure that the effective resistance of the parallel combination of R_{REF1} and R_{REF2} presents a low impedance to ground, relative to the value of R_1.

Factors affecting resolution

Performance of a pressure-sensor system relates directly to its resolution. Resolution is the smallest increment of pressure the system can resolve. For example, a system that measures pressure as high as 10 kPa with 1% resolution can resolve pressure increments of 0.1 kPa. The voltage resolution of an 8-bit ADC with a 5V window (5V high reference voltage and 0V low reference voltage) is 5V÷255, or 19.6 mV. Many pressure-sensor systems have ADC interfaces. If the 8-bit system requires 1% resolution, the pressure sensor's span must be at least 19.6 mV÷1%, or 1.96V. For 0.5% resolution, the span must be 3.92V.

The greater the resolution the system requires, the greater the sensor's amplified span must be. A pressure sensor's

unamplified span is only 10s of millivolts. Therefore, you must design an amplifier to provide the minimum span that yields the desired resolution. If the amplifier has a fixed gain, any device-to-device variation in the sensor's unamplified span results in variation in the amplified span. For example, if the sensor's span variation results in an amplified span that's smaller than the system requires, the system resolution is not as high as desired.

If the sensor's span variation results in an amplified span that's larger than the system requires, the resolution is better than desired. However, the amplified span might saturate the amplifier near its supply rails. The span might also extend beyond the reference levels of the ADC. The ADC converts voltages above the high reference as 255_{10} for an 8-bit ADC and converts voltages below the low reference as 0_{10}. This digital clipping creates nonlinearities in the A/D conversion and in the overall system-transfer function.

A problem occurs if you want to design a fixed-gain amplifier that gives the desired resolution, does not violate the limits of the linear ranges of the op amps and ADC, and also accommodates the complete distribution of possible sensor spans. The same problem occurs with additional sources of variation: device-to-device variation, temperature effects in the sensor's span, and zero-pressure offset voltage. You must also consider any component tolerances for the voltage regulator and resistors.

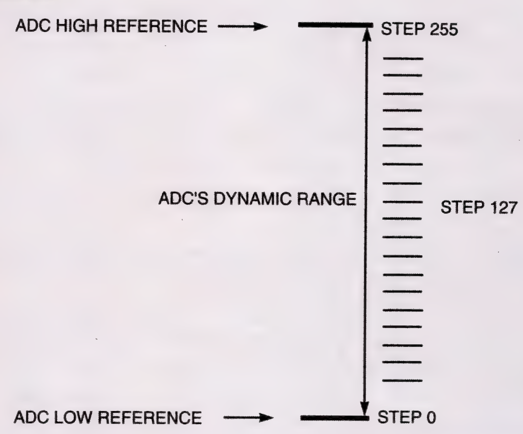
Designing a system that has only one source of variation is not difficult. However, the design becomes complicated when all the cited variations are interacting. This design method considers all the variations and interactions and uses worst-case limits to design a fixed-value system.

TABLE 2—MPX2010 PRESSURE-SENSOR VARIATION CHARACTERISTICS

Characteristic (V_S=5V)	Symbol	Minimum	Typical	Maximum	Unit
Pressure range	P_{OP}	0		10	kPa
Full-scale span	V_{FSS}	12	12.5	13	mV
Zero-pressure offset	V_{OFF}	–0.5		0.5	mV
Temperature effect on full-scale span (Note 1)	TCV_{FSS}	–1		1	%FSS
TC on zero-pressure offset (Note 2)	TCV_{OFF}	–0.5		0.5	mV

Notes:
1. Maximum change in full-scale span at 0 and 85°C, relative to 25°C.
2. Maximum change in offset at 0 and 85°C, relative to 25°C.

FIGURE 3



An 8-bit ADC produces digital outputs in 255 discrete steps.

Resolution vs headroom

The amplified span of the sensor must fit within the high and low references of an ADC to avoid any nonlinearity errors. The span must be large enough to provide the resolution the application requires. Headroom is any part of the ADC's window that's not used for the sensor's dynamic signal range. Headroom functions as a cushion between the high and low reference voltages and the sensor's dynamic output range. This cushion allows the sensor's dynamic range to move, or vary, within the ADC's window.

Fig 2 shows the relationship among the sensor's output span, the headroom, and the ADC's (or amplifier's) window. The total amount of sensor output-signal variation is from temperature effects, device-to-device variation, and interface-circuit component tolerances. This variation must not exceed the headroom available for the requisite system resolution. A large sensor span that uses more available bits for signal resolution results in a smaller amount of headroom to accommodate sensor-parameter and interface-circuit variations. A trade-off exists between resolution and variations. The more variation in the system, the more headroom the system requires for the variation. Consequently, less of the ADC's window is available for the sensor's true-signal span. Less span results in poorer resolution—fewer bits for resolving the sensor's output signal.

The method starts by defining all the known parameters. Parameters with an asterisk (*) are specified at 25°C. The parameters are

Resolution	Desired system resolution
MaxFSS*	Maximum full-scale voltage span of the pressure sensor,
MinFSS*	Minimum full-scale voltage span of the pressure sensor,
TCV_{FSS}	Maximum TC of the sensor's full-scale voltage span

FIXED-VALUE SENSOR SYSTEMS

MaxSensOff*	Maximum zero-pressure offset voltage of the pressure sensor
MinSensOff*	Minimum zero-pressure offset voltage of the pressure sensor
TCV_{OFF}	Maximum TC of the offset voltage of the pressure sensor
V_{LO}	Low saturation level of the amplifier or low reference voltage of an ADC (whichever is more limiting)
V_{HI}	High saturation level of the amplifier or high reference voltage of an ADC (whichever is more limiting)
V_{REF}	Reference voltage for positive dc-voltage level shifting
V_{TOL}	Voltage-regulator tolerance
MinTemp	Minimum operating temperature
MaxTemp	Maximum operating temperature.

These parameters are either specific to the application, such as system resolution, or appear in the sensor's data sheet. **Tables 1** and **2** provide the parameters for the two designs. The data in **Tables 1** and **2** represent a 5V supply voltage. The data sheets for the MPX10 and MPX2010 give specs for 3 and 10V supplies, respectively.

Apply the following steps to the MPX10 (example 1) and MPX2010 (example 2):

Step 1. Determine the required resolution in percent of full-scale output for the system.

Step 2. Calculate the number of steps the chosen resolution requires. The resolution sets the number of steps into which to break the pressure signal. (Note **Fig 3**, which assumes an 8-bit ADC with 255 steps of resolution.) A conservative way to determine the number of steps is to assume that for an ADC the digital quantization of the pressure signal can be within plus or minus one step. Therefore, assume that you need twice the number of steps previously determined to resolve a given minimum incremental signal. Thus, the number of steps for the chosen resolution is 2·100÷resolution. The scaling factor of 100 in the numerator converts the resolution from a percentage to a decimal.

Step 3. Evaluate the minimum amplified-sensor span. (The minimum required span is the minimum span that satisfies the resolution requirement (**Fig 4**).) Assuming the use of an 8-bit ADC with a 5V window, in which one step equals 19.6 mV with nominal regulator voltage, the minimum amplified sensor span equals the number of steps times 19.6 mV.

Step 4. Compute the amplifier's gain. The gain must be high enough over the entire distribution of sensor spans to achieve the minimum required span. Therefore, you calculate this gain using the smallest pressure-sensor voltage span, MinFSS. Using the smallest, worst-case sensor-voltage span to calculate the gain guarantees the minimum required span for the entire distribution of sensor spans. The worst-case minimum full-scale sensor span occurs at the highest temperature, MaxTemp, because the span decreases with increasing temperature (TCV_{FSS} is negative). The following equation shows the worst-case minimum:

$$\text{Gain} = \frac{\text{Minimum required span}}{\left[\text{MinFSS}\right] \bullet \left[1 + TCV_{FSS} \bullet (\text{MaxTemp} - 25)\right]},$$

where the term $[1+TCV_{FSS}]\cdot(\text{MaxTemp}-25)]$ is the temperature effect on the span.

In Steps 1 through 4, the calculations reflect a minimum desired resolution. The resolution requirement determines the number of steps into which to break the signal. This number of steps, multiplied by the number of millivolts per step, equals a minimum voltage range, or minimum required span. Finally, to ensure that you obtain this minimum required span over the entire distribution of sensor spans, calculate the gain using the worst-case smallest sensor span. (The gain varies because of resistor tolerances in the amplifier circuit. To ensure that tolerance-induced system variation is negligible in comparison with other sources of variation, you should design the system with resistors of 1% tolerance or better.)

TABLE 3—THE MPX10 PRESSURE SENSOR

Given parameters	Performance parameters	Headroom parameters
MaxFSS 83 mV at 25°C	[1]Resolution (%FSS) 4.5	[7]Maximum temp effect on offset 0.03V
MinFSS 33 mV at 25°C	[2]Number of steps 44	[8]Maximum offset variation 1.76V
TCV_{FSS} –0.22 %FSS/°C	[3]Minimum required span 0.87V	[9]Minimum offset –0.03V
MaxSensOff 58 mV at 25°C	[4]Gain 29	[10]Maximum offset 1.73V
MinSensOff 0 mV at 25°C	[5]Maximum span 2.57V	[13]V_{REF} 0.23V
TCV_{OFF} ±15 μV/°C		
V_S 5V	[6]Calculated headroom 1.78V	[11]Required headroom 1.75V
V_{HI} 4.8V		
V_{LO} 0.2V		[12]Is calculated headroom ≥required headroom?
V_{TOL} 5%		
MaxTemp 70°C		
MinTemp 0°C		

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Step 5. Calculate the maximum span—the largest possible span (**Fig 4**). You calculate the span by using the maximum full-scale sensor span, MaxFSS, and the gain. The worst-case maximum full-scale sensor span occurs at the lowest temperature, MinTemp. After you calculate the maximum span, the remaining dynamic range within the ADC's window or the saturation levels of the amplifier is the lowest number of bits (most limiting case) available for headroom. The following equation defines the maximum span:

$$[\text{Gain}]\cdot[\text{MaxFSS}]\cdot[1+TCV_{FSS}\cdot(\text{MinTemp}-25)],$$

where $[1+TCV_{FSS}\cdot(\text{MinTemp}-25)]$ is the temperature effect on the span.

Step 6. Compute the calculated headroom (**Fig 5**), which reserves bits in the ADC's dynamic range only for the variation arising from the sensor's zero-pressure offset voltage. In general, headroom is reserved for all sources of variation: system components, resistor tolerances (if significant), and the sensor. However, you should reserve the largest part of the headroom for the device-to-device variations and temperature effects on the sensor's zero-pressure offset voltage.

The sources of variation from the other system components subtract immediately from the headroom so you can focus on the sensor-related variations. (This subset of the total headroom is the calculated headroom.) The following expression gives the calculated headroom:

$$5\bullet\left(1-\frac{V_{TOL}}{100}\right)-2\bullet V_{LO}-\text{Maximum span.}$$

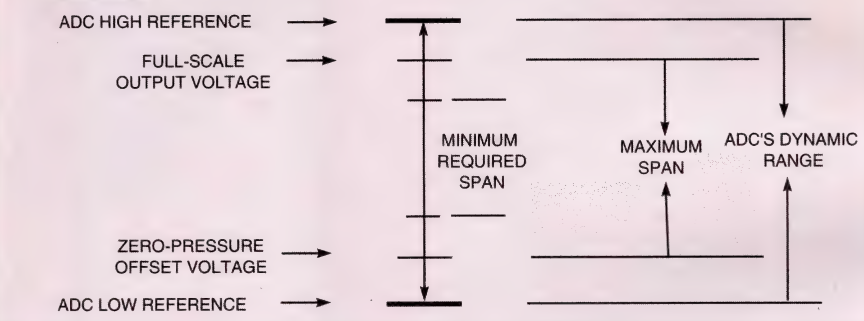
This equation assumes the difference between V_{HI} and the high supply rail, or high reference of the ADC, equals the difference between V_{LO} and the low supply rail, or the low reference of the ADC; thus, the term: $2\cdot V_{LO}$).

Step 6 is pivotal because it makes the transition from the performance requirements to the headroom requirements. Before Step 6, the method considered only the span of the sensor to guarantee a minimum resolution, despite device-to-device variation, component tolerances, and temperature effects. After determining the calculated headroom, the remaining steps consider the offset variations from device-to-device differences and temperature effects.

These offset variations add to form the required headroom (**Fig 6**). The required headroom is the number of bits the ADC's dynamic range needs to accommodate the offset variations. You compare this required headroom with the calculated headroom to determine if the calculated headroom can allow for the offset variations. The calculated headroom must be greater than or equal to the required headroom. If not, you must relax the resolution requirement or reduce the variations rising from offset, span, or component tolerances (or all three).

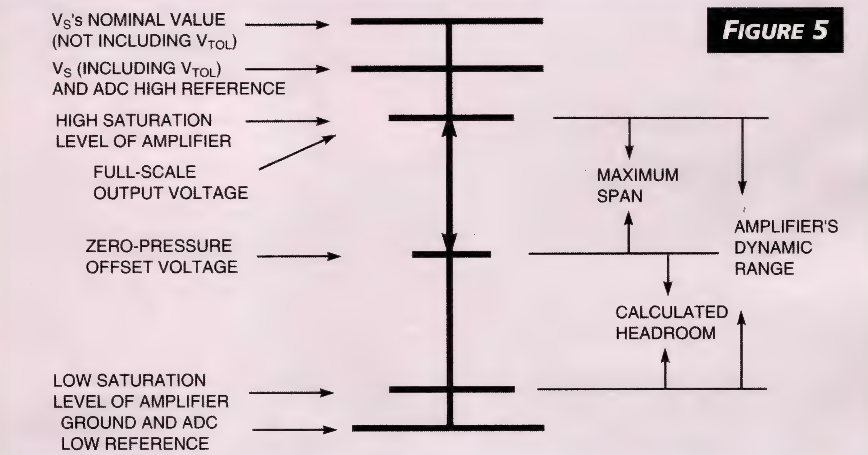
Step 7. Calculate the maximum offset drift, the maximum temperature effect on offset in **Fig 6**, rising from temperature fluctuations. A conservative approach is to determine the maximum total voltage change over the entire operating-temperature range. This maximum offset change is the product of the amplifier gain, TCV_{OFF}, and the entire operating-temperature range, from MaxTemp to MinTemp. Because the TC of offset can be positive or negative, the offset may increase or decrease with increasing temperature. Although this step considers only the maximum magnitude of the temperature-induced change in offset, a segment in the required headroom is reserved for both possibilities: a positive or negative TC offset (**Fig 6**). The maximum temperature effect on offset is

FIGURE 4



The ADC's resolution and dynamic range determine the minimum required amplified sensor span.

FIGURE 5



You must reserve a section of voltage for each source of variation from ground to the supply voltage.

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[Gain]·[TCV_{OFF}]·[MaxTemp–MinTemp].

Step 8. Determine the maximum offset variation (**Fig 7**). This parameter is the total amount of required headroom that you must reserve for the entire distribution of sensor offsets at room temperature. To determine the maximum offset variation

[Gain]·[MaxSensOff–MinSensOff],

where the largest offset is Gain·MaxSensOff and the smallest offset is Gain·MinSensOff.

Step 9. Calculate the worst-case minimum offset (**Fig 7**). This parameter uses both temperature effects from Step 7 and device-to-device variations from Step 8 to determine the smallest possible offset over the entire distribution of sensor offsets and the operating-temperature range. This worst-case minimum offset occurs when a sensor has a nominal room-temperature offset of MinSensOff and a negative TC, so that the offset decreases with increasing temperature. MinSensOff is the smallest offset in the sensor-offset distribution. The following expression defines the minimum offset:

[Gain]·[MinSensOff]–maximum temperature effect on offset.

Step 10. Compute the worst-case maximum offset (**Fig 7**). This parameter uses both temperature effects from Step 7 and device-to-device variations from Step 8 to determine the largest possible offset over the entire distribution of sensor offsets and the operating-temperature range. This worst-case maximum offset occurs when a sensor has a nominal room-temperature offset of MaxSensOff and a positive TC, so that the offset increases with increasing temperature. MaxSensOff is the largest offset in the sensor-offset distribution. The following expression defines the maximum offset:

[Gain]·[MaxSensOff]+maximum temperature effect on offset.

Step 11. Determine the required headroom (**Fig 7**), which is the difference between the maximum and the minimum offset. This parameter is also the amount of voltage range (in bits of the ADC) the system requires to allow for device-to-device and temperature variations of the sensor's offset. The equation for the required headroom is

Maximum offset–Minimum offset.

Step 12. Compare the required headroom of Step 11 with the calculated headroom of Step 6. The calculated headroom is the absolute amount of offset variation rising from device-to-device variations and temperature effects that the system can allow for the desired resolution. If the required headroom is greater than the calculated headroom, the desired resolution is not attainable for all worst-case variations from temperature effects, component tolerances, and device-to-device variations. The requirement to attain the desired system resolution is:

Calculated headroom≥Required headroom.

If your system does not meet this requirement, you can take the following actions:

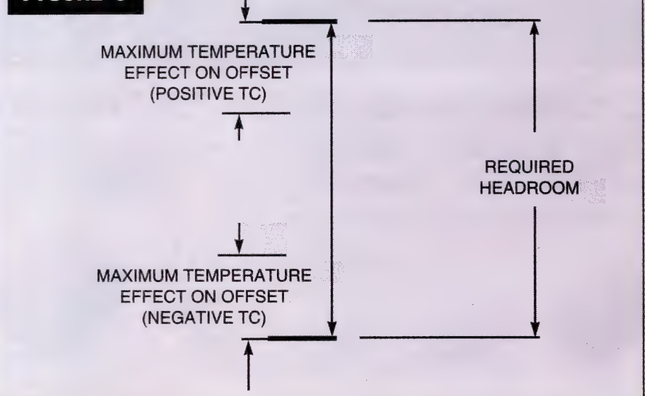
- Relax the resolution requirement, and repeat the method;

(continued on pg 95)

TABLE 4—THE MPX2010 PRESSURE SENSOR

Given parameters	Performance parameters	Headroom parameters
MaxFSS 13 mV at 25°C	[1]Resolution (%FSS) 1.2	[7]Maximum temp effect on offset 0.14V
MinFSS 12 mV at 25°C	[2]Number of steps 167	[8]Maximum offset variation 0.55V
TCV_{FSS} ±1 %FSS°C	[3]Minimum required span 3.27V	[9]Minimum offset –0.27V
MaxSensOff 0.5 mV at 25°C	[4]Gain 275	[10]Maximum offset 0.27V
MinSensOff –0.5 mV at 25°C	[5]Maximum span 3.61V	[13]V_{REF} 0.47V
TCV_{OFF} ±0.5 mV, 0 to 85°C		
V_S 5V	[6]Calculated headroom 0.74V	[11]Required headroom 0.55V
V_{HI} 4.8V		
V_{LO} 0.2V		[12]Is calculated headroom ≥required headroom?
V_{TOL} 5%		
MaxTemp 85°C		
MinTemp 0°C		

FIGURE 6



You must reserve segments in the required headroom for both positive and negative TCs of zero-pressure offset.

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- Reduce (tighten) the span or offset (or both), and repeat the method;
- Reduce the TCs, and repeat the process;
- Reduce the component tolerances, and repeat the method; or
- Perform a combination of the above actions, and repeat the method.

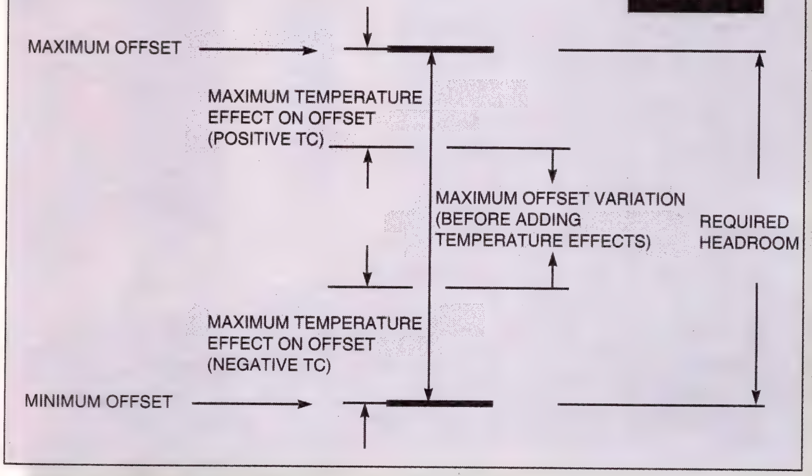
Step 13. You need a dc offset, V_{REF}, to position the sensor's span within the ADC's window. This offset ensures that no device-to-device, temperature variation, or component tolerances cause the sensor's output to fall outside the window. Therefore, calculate the V_{REF} required to ensure that the sensor's smallest zero-pressure offset voltage (minimum offset) is greater than or equal to V_{LO} (**Figs 5** and **7**). The sum of the reference voltage and minimum offset must be greater than or equal to the amplifier's low saturation voltage, as the following equation shows:

$$V_{REF}+\text{Minimum offset}\geq V_{LO}.$$

To solve for V_{REF}

$$V_{REF}\geq V_{LO}-\text{Minimum offset}.$$

FIGURE 7



The temperature effects of Fig 6 combine with device-to-device variations to determine the worst-case offset conditions.

The reference voltage, V_{REF}, has variations from the tolerances of the resistors in the divider that create V_{REF}. To ensure that the system variation from resistor tolerances is negligible in comparison with other sources of variation, you should design the system using resistors having 1% tolerances or better.

Executing the method

Tables 3 and **4** contain designs using the MPX10 and MPX2010 pressure sensors, respectively. The cell headings in the tables correspond to the designs in the text. In addition, the bracketed numbers next to the cell headings are the steps in the method. The first column lists the parameters that should be available in, or derived from, the data sheets for the appropriate components: sensor, amplifier, voltage regulator, and resistors.

The second column lists the performance requirements of the sensor system. This column lists the calculations for a minimum sensor span that you need to obtain the desired resolution, despite device-to-device variations, temperature effects, and component tolerances. The third column lists the calculations that determine the headroom for the system, the given component tolerances, the sensor-offset device-to-device variations, and the temperature effects. You can easily implement the table and design equations into a spreadsheet to efficiently perform the required calculations.

Tables 3 and **4** show how sources of variation can affect the overall system resolution. The MPX2010 has on-chip temperature-compensation and calibration circuitry to reduce device-to-device variations and temperature effects. Consequently, when you design the fixed-value amplifier system, the possible resolution with the MPX2010 is almost four times greater than the resolution from the amplifier circuit using an MPX10. In each example, the method optimizes the system resolution, taking account of the sensor device variations and other component variations.

This method does not address how to obtain the best performance from a single sensor system. Instead, the focus is on obtaining the best possible system performance while considering the distribution of device parameters that result from manufacturing and other sources of variation. By considering the sources of variation, you can mass-produce the system without individually calibrating the sensor-system hardware. If the system's calculations show that the sensor's signal is within the dynamic range of the amplifier and the ADC, you can implement a software calibration to nullify any room-temperature device-to-device and component variations. EDN

Authors' biographies

Eric Jacobsen is a systems and applications engineer for Motorola's Sensor Products Division, Phoenix, where he has worked on product and system design and customer support for three years. He holds a BSEE from the University of Illinois, Urbana/Champaign, and is pursuing an MSEE at Arizona State University, Tempe, AZ. His hobbies include music and audio equipment.

Jeff Baum is a systems-engineering manager at Motorola's Sensor Products Division, Phoenix, where he's worked for five years. He defines new products, develops system-level sensor circuitry, and designs new-product prototypes. A member of Eta Kappa Nu, Baum holds a BSEE from the University of Illinois, Urbana/Champaign, and an MSEE from the University of Arizona, Tucson, AZ. His hobbies include travel, studying Japanese, and combat-pistol shooting.

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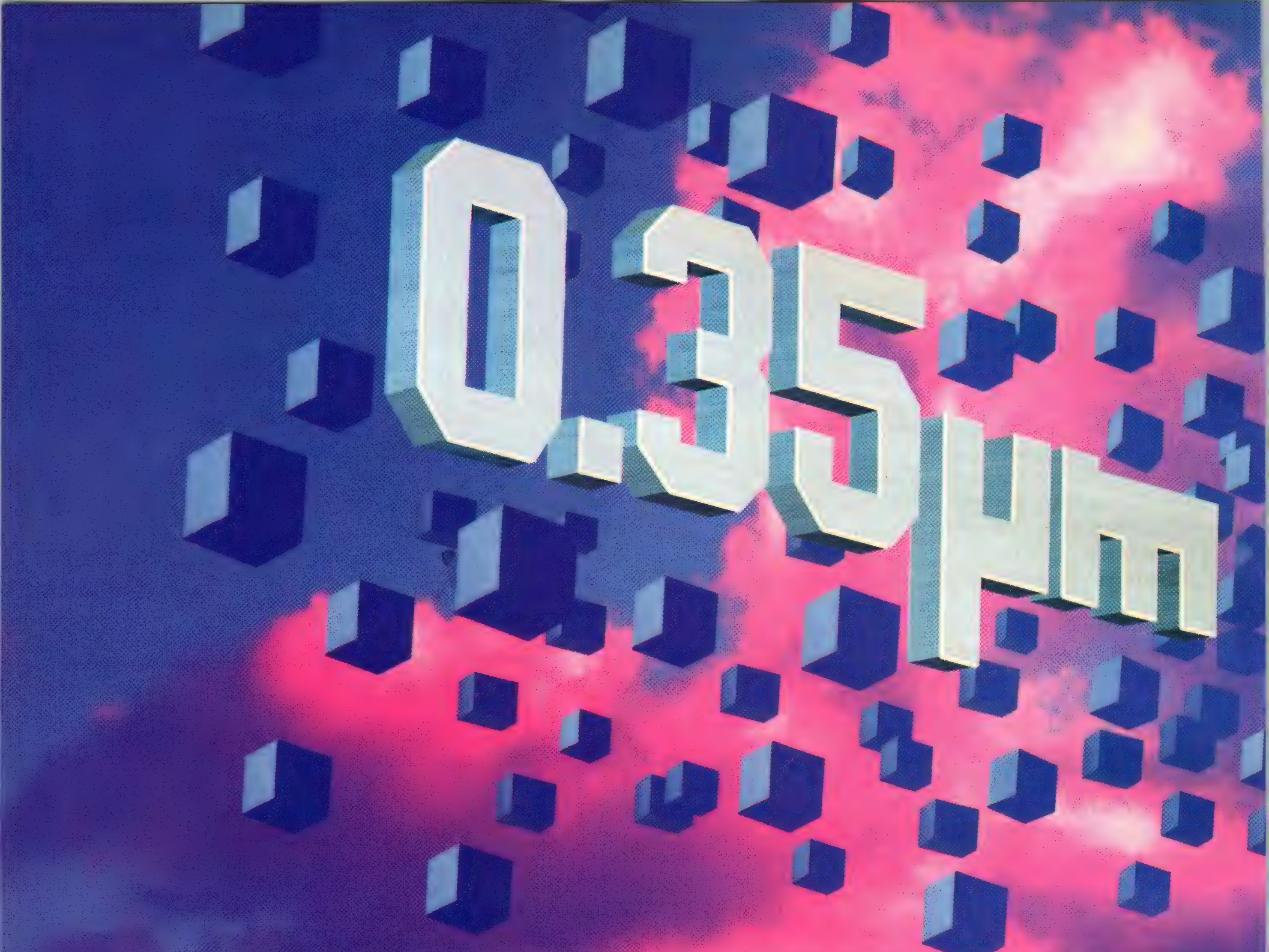

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03602-122-09220	5x7 dot matrix	2x20	9mm	7.75″	2.58″	1.00″	675mA
03602-124-09420	5x7 dot matrix	4x20	9mm	7.75″	3.40″	1.00″	1300mA
03702-020-05220	14-segment	2x20	5mm	5.65″	1.98″	0.82″	270mA
03702-021-08110	14-segment	1x10	8mm	5.00″	1.60″	0.90″	140mA
03702-022-13112	14-segment	1x12	13mm	7.20″	2.40″	0.90″	323mA
03702-024-09116	14-segment	1x16	9mm	6.70″	2.30″	0.90″	360mA
03702-026-09120	14-segment	1x20	9mm	8.30″	2.35″	0.95″	390mA
03702-029-13120	14-segment	1x20	13mm	10.20″	1.93″	0.96″	526mA

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Cryptography is key to securing proprietary information

ANTONY WATTS, SGS-THOMSON MICROELECTRONICS

Computer and communications technologies are converging. Satellite and cable TV, electronic mail, and smart bank cards are among the slew of applications involved. Some applications routinely risk transmitting valuable information over low-security channels. By using cryptography, however, you can encode proprietary data and prevent its misuse.

It's no secret that digital information has become a hot commodity. Because of increased demands for electronic information and the corresponding growth in value of this data, companies are stepping up security efforts. Telephone companies have deemed simple security mechanisms, such as fuses and transport codes, sufficient for applications such as prepaid telephone cards. But consumers and retailers are demanding more sophisticated security for applications involving credit cards, electronic mail, electronic cash, and home banking. "Cryptography" technology, which is the science of encoding and decoding messages, makes new levels of electronic security now viable for mass-market applications.

Cryptography is not a new subject for the semiconductor industry; microprocessors have implemented schemes such as DES (Data Encryption Standard) for more than 20 years. However, the secret-key cryptographic technique upon which DES is based is now being challenged by public-key cryptography, which offers major advantages in many applications.

Growing interest in smart bank cards, "electronic purses," and home-banking systems also raises security concerns. For example, a customer can use a home terminal to instruct the bank to pay bills by transferring money from one account to another. In this transaction, electronic security involves ensuring that the customer's message will not be intercepted—and the identity of the payee altered. Similarly, the bank must be able to prove that the payment request was indeed sent by the customer (and that the message was not altered during transmission). A security system must also protect against a technique known as "replay," where a genuine message (for example, one that instructs the bank to pay a certain sum into an account) is recorded and sent again and again.

The most common security threats include the following:

- **Interception**—passive eavesdropping
- **Replay**—genuine messages that are recorded and resent
- **Masquerade**—receiving a message from a source other than the source the message claims
- **Repudiation**—receiving a message that the sender later denies sending
- **Manipulation**—intercepting and modifying messages for fraud or industrial sabotage.

To protect against these threats, a cryptographic system must offer three features:

- **Secrecy**—to protect message privacy from anyone without an appropriate key to decipher encrypted messages
- **Integrity**—to allow detection of whether a message has been altered
- **Signature**—to establish sender identity and prove that an individual sent the message.

Cryptographic systems

All practical cryptographic systems operate in the same basic way. An encryption algorithm and key convert an original message, "plain text," into a coded message, "cipher text." A decryption algorithm and key are necessary to decode the cipher text. Security and secrecy normally reside in the keys, not in the algorithms, because using standard algorithms has clear commercial benefits. In fact, cryptographers usually act on a worst-case assumption that the entire mechanism of encryption is known to all parties, which is called Kerckhoff's Assumption.

Cryptographic schemes fall into two distinct groups: secret-key and public-key methods. **Fig 1** illustrates the secret-key system. The secret-key algorithm is fully reversible

and symmetric; decrypting the cipher text yields the original plain text.

The most widely used scheme of this kind is DES, which breaks plain text into 64-bit blocks and encrypts each block using a 56-bit secret key to generate a 64-bit block of cipher text. You must use the same key to recover the original text from the cipher text.

Encoding data is sufficiently complex to ensure that even the most powerful computers currently available would take more than 100 years to break the code. Unfortunately, anyone who knows the key can decode the message. In addition, there is no way of ascertaining whether the decoder is supposed to know the key. Similarly, although it is possible to use hash functions to add integrity checks to the message, the value of this move is undermined by the lack of a signature facility.

FIGURE 1

HOW A SECRET-KEY SYSTEM WORKS:

Scoring high marks

Secret-key systems score high marks in secrecy but perform poorly in other applications. These systems are also impractical in situations where many potential pairs of senders and receivers need to agree on a unique key to communicate. The unique key is not a problem in banking applications, because the bank can issue the keys in the same way as conventional PINs (personal-identification numbers). In e-mail systems, on the other hand, the number of keys can approach the number of users squared.

Public-key systems (**Fig 2**) are asymmetric; the encryption and decryption algorithms are different, so passing the cipher text through the encryption stage again does not yield the original message. For public-key systems, you need one key for encryption and another key for decryption. Although these keys are mathematically related, it is possible not only to devise algorithms that allow the encryption key to be distributed publicly, but also to prevent discovery of the decryption key from this knowledge (**Ref 1**).

To send a message using a public-key system, the sender looks up the recipient's encryption key in a public directory and uses this to encrypt the message. He can then send the

cipher text using an insecure communications method, such as the public-telephone system. The recipient then decodes the message using his secret decryption key.

Public-key systems have two important benefits. The first is that you have to remember only your own decryption key, which greatly simplifies key distribution and management. The second benefit is that public-key systems offer the ability to implement "electronic signatures," a particularly important feature in applications such as home banking and electronic mail.

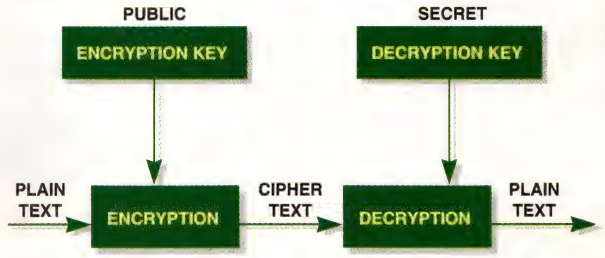
De facto standards

Although there are no international standards for public-key cryptosystems, de facto standards, such as RSA (named after Rivest, Shamir, and Adelman, who published their algorithm in 1977), have emerged. You can use public-key systems without knowledge of the underlying mathematics, but the following simplified description of the RSA method illustrates the encryption and decryption processes. For this example, the message is a 512-bit number, equivalent to a block of 64 conventional 8-bit ASCII characters. Longer messages are encrypted in 512-bit blocks.

Suppose you choose two very large prime numbers, P and Q, and another very large number, d, which is relatively prime to (P–1)*(Q–1). Then calculate e, the unique number that satisfies the equation e*d=1 [mod ((P-1)*(Q-1))]. The pair of numbers (e, N), where N is congruent to P*Q, is the encryption key; the number pair (d, N) is the decryption key.

FIGURE 2

HOW A PUBLIC-KEY SYSTEM WORKS:



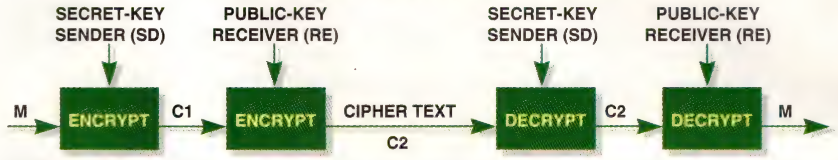
The encryption algorithm consists of raising the message to the power of e and taking the remainder when the result is divided by N. The result is the cipher text. Note that the same algorithm operating on the cipher text as the input and d instead of e as the exponent yields the original message (**Ref 2**).

Although the encryption key (e, N) uniquely determines the decryption key (d, N), potential hackers can compute d only if they know the prime factors, P and Q, of N. Breaking the code is equivalent to finding the prime factors of the

CRYPTOGRAPHY

number N; you can make the time required to do this arbitrarily large by a suitable choice of P and Q. Typical public-key systems use prime numbers with 100 digits or more; with numbers of this size, the chance of success using any known factoring algorithm is effectively zero. At the same time, readily available computer algorithms can rapidly calculate suitable values for P, Q, d, and e.

FIGURE 3 "SIGNING" MESSAGES USING A TWO-STAGE ENCRYPTION PROCESS:



Electronic signatures

One immediate advantage of public-key cryptography is that it eliminates key-management problems; a new member of a public-key system needs only to obtain a copy of the public directory and to distribute his chosen encryption key. However, you may opt to attach an electronic signature to a message.

Electronic signatures are possible in a public-key system because the distinction between encryption and decryption keys and algorithms is arbitrary. Provided that the equation e*d=1 [mod ((P-1)*(Q-1))] is satisfied, it makes no difference whether you chose e or d as the encryption key. This means that you can encode a message using the secret key that is normally used for decryption and decode the cipher text using the public key normally used for encryption.

As **Fig 3** shows, you can sign an electronic message using a two-stage encryption. First, encode the message using your secret key, SD, to generate an intermediate cipher text, C1. This step provides no protection by itself because the decryption key is freely available in the public directory. Following the first encryption by a second encryption using the receiver's public key, RE, to generate the cipher text allows you to transmit the encrypted and safe data over an open communications channel.

On receipt of the cipher text, the receiver can use his secret key to decrypt the message. However, instead of the message, decryption yields the intermediate cipher text. The receiver can then decrypt the message with the public key. As a result, the receiver has the original message and the sender's signature. This method protects against masquerade and repudiation threats. The signature exists because you created a signed message by encoding with your secret key.

Additional safety features

A third party can send a message purporting to be from you only if that party knows your secret key. If the third party uses any other key, the final decryption stage using SE will generate gibberish. Similarly, you cannot deny having sent the message because a message that decodes successfully with your public key must have been originally encoded with your secret key.

By using hash functions and adding date and time data to messages before encrypting, you can provide complete protection against replay and manipulation threats. Public-key systems thus satisfy all of the major cryptographic requirements; many organizations, including the US National Institute of Standards and Technology, the American Bankers Association, and the French Banking Association, have accepted the technique.

Despite the significant advantages available with public-key cryptography, secret-key systems have enjoyed far greater use. Public-key algorithms require considerably more computational resources to match the encryption/decryption speeds of secret-key systems. These resource requirements have led to unacceptably high costs.

Secret-key cryptography requires a CPU to perform modular exponentiation in the equation: M is congruent to Cd (mod N). Traditionally, this operation involves multiplying a number by itself, dividing the result by N to give a quotient, subtracting N*quotient from the number squared, and repeating the sequence d times. The division operation is particularly undesirable because it is the slowest of the basic arithmetical operations.

With the discovery of algorithms that perform modular exponentiation without division (**Ref 3**), CPUs can speed computations. EDN

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Author's biography

Antony Watts holds a degree in Solid State Physics from London University. He currently works as communication director for the Memory Products Group of SGS-Thomson Microelectronics.

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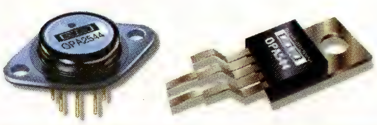

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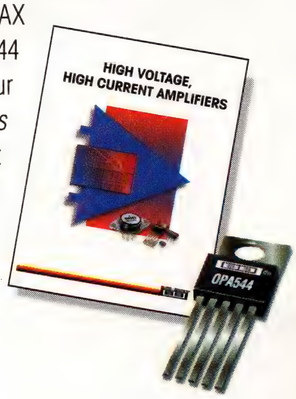

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Options dot the programmable-logic landscape

RICHARD KAPUSTA, CYPRESS SEMICONDUCTOR CORP

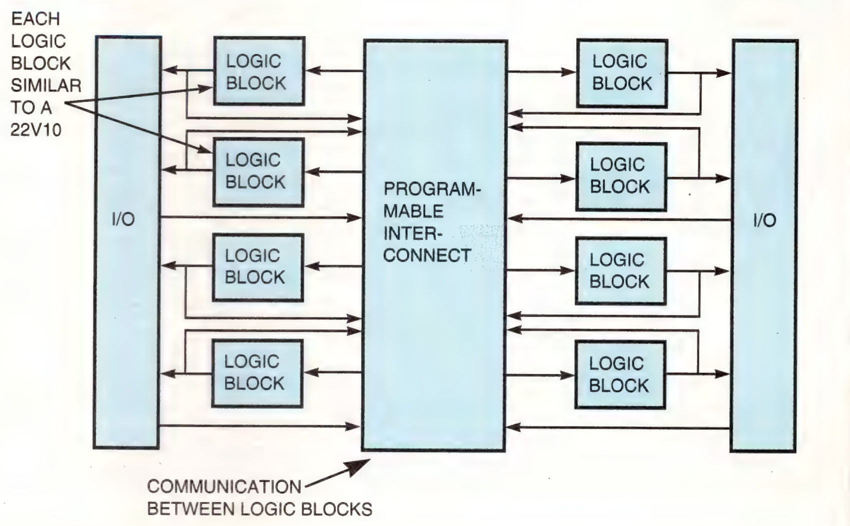
PLDs have emerged as indispensable tools for system designers. They have evolved from fast prototyping tools into production devices that quickly get your designs to market, when anticipated volumes don't justify the cost of a full ASIC design.

When contemplating the use of PLDs, you face an array of options. Each PLD type has a unique set of characteristics that bring advantages and disadvantages to any design. Knowing how to sort out these differences is essential to creating efficient, cost-effective designs that wring the highest possible performance out of the devices.

Three major PLD types are in use, each with a distinct architecture, capacity, and performance capability:

- A simple PLD comprises a single logic block. It is restricted in the amount of logic that can be implemented. The industry-standard 22V10 is such a device. It has 12 dedicated inputs, a product-term array, a product-term allocation scheme, 10 macrocells, and 10 I/O cells.
- A complex PLD (CPLD) comprises multiple logic blocks that communicate with one another through a global interconnect (**Fig 1**). Each logic block in a CPLD is similar to a simple PLD, containing inputs, a product-term array, a product-term allocation function, macrocells, and I/O cells. These elements connect to build desired logic functions. The number of macrocells and inputs and the method of allocating product terms vary with vendors' product families.
- A field-programmable gate array (FPGA) is a collection of logic cells that communicate with each other and with I/O pins via horizontal and vertical routing channels (**Fig 2**). Functions are built by connecting the logic cells. The logic contained within FPGAs is typically more versatile or fine-grained than that of simple PLDs or CPLDs. However, the flexibility of FPGAs comes at a price; FPGAs cannot provide fixed delays, so they are more complicated to use.

FIGURE 1



In a CPLD such as the Flash370, logic blocks and I/O pins communicate with each other through the programmable interconnect.

- A PLD's capability depends on resources such as its approach to interconnect—the way in which it routes signals between logic blocks and I/O pins. In CPLDs, interconnects can occur in two ways:
- In a full crosspoint switch configuration, typified by the Cypress MAX340 family. Such an interconnect is completely routable; that is, any combination of simultaneous signals can be routed to or from any logic block through the global interconnect. However, this arrangement is slow and large: The 100% crosspoint-switch-based interconnect sacrifices speed and die size for maximum flexibility of signal placement and design modification.
- A multiplexer-based approach, typified by the Cypress Flash370 CPLD family and used by many vendors. Distributing all signals through multiplexers instead of a crosspoint-switch system reduces interconnect size and enhances speed. There are many implementations of multiplexer-based interconnects, and the ultimate routability of a multiplexer-based scheme varies from vendor to vendor. The Cypress Flash370 CPLD family provides much higher performance than CPLDs based on the crosspoint switch and provides a highly routable interconnect.

Routability involves two aspects. First is the number of signals the global interconnect provides into each logic block. If the maximum number of signals that can be routed to a logic block is smaller than the required number for a particular logic function, then the design will not fit or will have to be partitioned among multiple logic blocks.

The second aspect is the routability within the interconnect itself; that is, the probability of finding an interconnect that routes all the required signals into the appropriate logic blocks.

Two factors make finding such an interconnect difficult. First, as the number of signals that must be routed into a logic block approaches the maximum, it becomes much more difficult to find a way to interconnect the signals. Second, as you begin to fix the input location of these signals, it becomes harder to route them to the appropriate logic blocks.

Additional problems can arise in some CPLDs if their design requires logic changes after a pinout produces a successful route. With the changes, the design may no longer fit with the same pinout. Some architectures feature better interconnect routability than others, and you should carefully consider routability as you select your device.

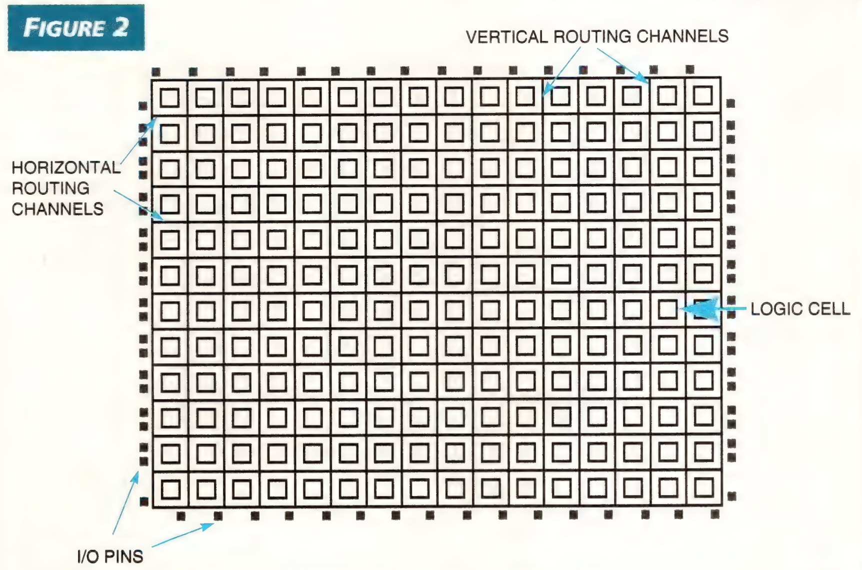
After interconnect, the second major resource to consider in evaluating a PLD is the characteristics of the logic blocks themselves, such as their ability to perform logic on a given number of inputs. Logic-block capabilities have evolved since the introduction of the now-ubiquitous simple PLD, the 22V10. This device has a fixed number of product terms available to each macrocell, designated by the numbers 10, 12, 14, and so on. If you use fewer product terms than the designated capacity of a macrocell, you lose the rest because you cannot steer them to another macrocell. Furthermore, multiple macrocells cannot share a product term, so you must duplicate this logic at every macrocell that requires it. The concepts of steering and sharing are important because they permit more efficient utilization of device resources and enhance performance.

As CPLDs emerged, vendors attempted to implement product-term steering and sharing. With product-term steering in many early CPLDs, designers moved a group of logic from an adjacent macrocell when a function required more product terms than those allocated to a macrocell. This movement increases the amount of logic available to that macrocell, but it also strands the adjacent macrocell with no logic, reducing the overall utilization of the CPLD and resulting in wasted resources because no logic is available for them.

The product-term sharing that many CPLDs use allows you to implement logic once and use it multiple times in generating other more complex functions. The basic problem in most implementations of this scheme is the added signal delay using these shared resources incurs.

The most advanced CPLDs employ a method in which software steers and shares single product terms as needed without stranding macrocells or incurring any extra delay (**Fig 3**).

FIGURE 2



Horizontal and vertical routing channels and I/O pins appear along the periphery of this pASIC380 FPGA.

Capabilities of FPGAs

The architecture of an FPGA differs widely from that of a CPLD. Instead of a global interconnect matrix, the logic cells of an FPGA communicate with one another via vertical and horizontal routing channels. A typical FPGA logic cell is smaller and less complex than

that of a CPLD. The cell usually comprises a register with associated logic and has multiple inputs and outputs (**Fig 4**).

An FPGA design typically employs an I/O pin, one or more logic cells, an optional register, and another I/O pin leading off the chip. The delays imposed by the wire and programmable elements, the number of cascaded logic cells, and the propagation delay of each logic cell determine the ultimate design performance. The capacity depends upon the flexibility inherent in the logic cells and the routability of the interconnect.

An FPGA's technology impacts both the interconnect delay and the routability. The two major types of FPGA technologies are SRAM- and antifuse-based. The smaller size of the antifuse interconnect permits many more programmable elements to fit on a chip of comparable size and density. An SRAM-based FPGA, with fewer possible interconnects, is more restricted in its routability than an antifuse-based FPGA. On the other hand, an SRAM-based FPGA has the advantage of reconfigurability, a feature that some applications require.

SRAM- and antifuse-based FPGAs also differ in their logic-cell architecture. Although no logic-cell configuration is inherently better than another, the two architectures are distinguished by whether they are fine- or coarse-grained. Antifuse FPGAs typically use the fine-grained approach, which involves quite small and relatively simple logic cells. You have to use more logic cells to implement a function than you would to implement an equivalent function with a coarse-grained FPGA. Thus, a fine-grained approach relies more heavily on the interconnect and multiple cascaded cells, which may slow performance.

However, if the interconnect and logic cells are inherently fast, delays aren't a problem. Alternatively, with SRAM-based FPGAs, you must minimize interconnect because of the higher delay and fewer fuses available, thereby limiting your routing choices.

Selecting the right device

Your choice of PLD may involve several trade-offs. For example, the smallest PLDs are usually the fastest. However, they are also the least dense and may not be able to accommodate your design in one device. The maximum rating of a 22V10 can vary from vendor to vendor, but the leading edge today is approximately 175 MHz, corresponding to about a 4-nsec delay from input to output. A CPLD works better in more complex designs because it is somewhat like having many smaller PLDs on one chip.

For a 7.5-nsec delay, CPLDs can reach approximately 150 MHz. For some CPLD families, taking advantage of various architectural features affects design performance, and the maximum performance rating of a device applies only to the simplest of designs. In other words, make sure that a CPLD with a 7.5-nsec input-to-output delay in its data sheet will perform your design at that speed before you make your decision.

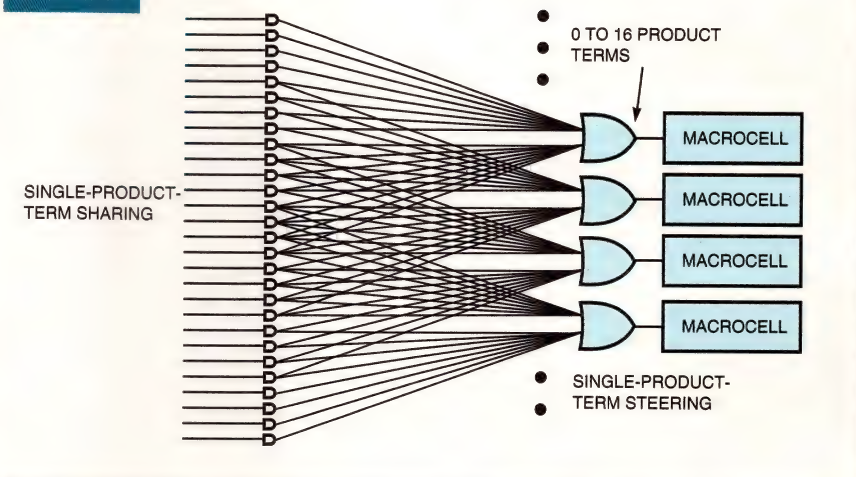
The story is different for FPGAs. It is difficult to provide specifications for parameters such as propagation delay and maximum frequency because they depend completely on the placement and routing of the design. An absolute timing prediction is, therefore, impossible. An FPGA is generally slower than a CPLD or simple PLD, depending on the application. In terms of density, FPGAs are the largest devices in the PLD spectrum.

The ease of predicting design performance based on the manufacturer's data-book specifications is also an important concern. Predictability is tied closely to the general ease of use of each PLD family. As a rule of thumb, the smaller the device, the more predictable it is. With a 22V10, you typically know in advance exactly what the performance will be.

CPLDs are somewhat less predictable but vary from family to family. Some CPLD families have specifications for timing delays that depend on factors like fan-out or the number of product terms. The software compiler ultimately makes these implementation decisions, forcing you to implement the entire design before knowing what the performance will be. Other CPLD families have more straightforward timing specifications and are, thus, much easier to use. Finally, FPGAs are the least predictable of PLDs: You must implement the design before knowing what the final performance will be.

To determine which device will meet your performance requirements, you can use the benchmarks provided by the Programmable Electronics Performance Corp (PREP) (see **box**, "Using the PREP benchmarks"). In addition to performance, though, consider the tools available for implementing the design (see **box**, "Design-tool considerations").

FIGURE 3



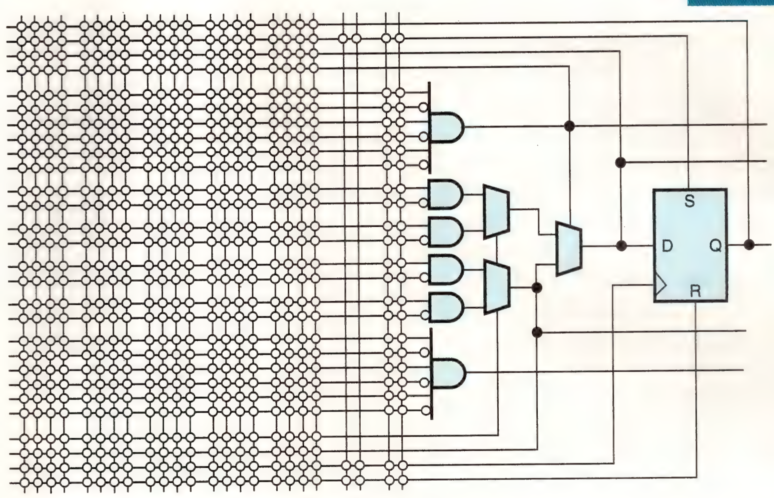
Product terms go to macrocells on an individual basis as the software requires in this Flash370 CPLD product-term allocator. As many as four macrocells can share a product term without performance penalty, eliminating the need to duplicate logic.

PROGRAMMABLE LOGIC DEVICES

Choosing a PLD based on density is a cut-and-dried decision. If your design calls for a certain capacity, your choice is circumscribed. The problem lies in determining the true capacity of a device. Two FPGA vendors may offer products listed as 4000-gate devices, but the actual densities they provide might differ widely.

The real question is, "How many gates are usable?" In a CPLD application, if your design contains signals with very complex logic, it may borrow logic from other macrocells, thus stranding macrocells throughout the device. The actual density available might be much smaller than the vendor-specified density. One way to get reasonable assurance of the actual density and whether your design will fit is to use the PREP benchmarks.

FIGURE 4



This fine-grained pASIC380 logic cell accommodates 23 inputs from routing channels and provides five outputs.

Power consumption is an important consideration in any design, especially with the current rapid growth of mobile communications and portable computers. Because the power a PLD consumes depends on the speed of operation and varies from vendor to vendor, it's difficult to create a guideline based on power alone. As a rule, for the same application, a CPLD consumes more power than does an FPGA. Typically, flash- or EEPROM-based PLDs require more power than SRAM- or antifuse-based devices.

State machines are among the most popular applications for programmable logic. Because CPLDs and FPGAs differ in architecture, the optimal state-machine implementation also differs. FPGAs have a register-intensive architecture, and the amount of logic per register is less than that of a CPLD.

(continued on pg 114)

USING THE PREP BENCHMARKS

In 1991, eight PLD vendors in association with programmable-logic users formed the Programmable Electronics Performance Corp (PREP) to provide a comparison standard for the relative capacity and performance of field-programmable gate arrays (FPGAs) and complex PLDs (CPLDs). The PREP members developed a suite of nine benchmark circuits to objectively evaluate the relative performance and capacity of the various devices in a design.

These benchmarks provide a means for comparing the relative impact of device architecture and technology implementation on performance and capacity. The actual implementation of each circuit is left to the device vendor, which implies that the reported results are the absolute best for each device. The functionality of each implementation must exactly match the PREP benchmark specification, and any user must be reproducible by any user.

The benchmark data quantifies the speed and logical capacity of the PLDs. You measure the capacity by instantiating the benchmark circuit multiple times in a single device until the device is filled. You calculate the performance by measuring the instance-to-instance performance for each repetition of the benchmark and then reporting the best, worst, and arithmetic mean of the internal clock-to-clock maximum frequency based on worst-case guaranteed device specifications. The external frequency also uses the clock-to-output specification and the external pin-setup time between the last instance and the first.

Each PREP member seeking PREP certification for a device must report benchmark data for all nine benchmarks in a standard format and submit them for verification and certification by a third party before publication of certified results. PREP itself cautions that, although benchmarks are important, they are not a substitute for data sheets, and they provide a limited view of device capabilities.

The benchmarks can be useful as a first-level, coarse screening in selecting a device, but keep benchmark limitations in mind. In most cases, the interconnection of multiple instances in a benchmark circuit is unlike the interconnections in real designs. As a result, the reported capacities for a device may be higher than actually available in a real design, and real design may exhibit slower performance than the benchmark because of denser interconnection.

Further, PREP does not endorse averaging data for a device across all nine benchmarks. Such averages in vendor data sheets can be misleading. In general, you cannot use the benchmarks to predict system design performance.

PROGRAMMABLE LOGIC DEVICES

Thus, you can take advantage of the inherent architectural edge of CPLDs by minimizing the number of registers your design requires.

In sequential state encoding, you assign each state a binary value starting with zero and progressing sequentially. In some very complex state machines, the amount of transition logic for a sequentially encoded state machine exceeds the maximum logic available in even the most sophisticated CPLDs, and you should use another state-encoding scheme.

Another architectural advantage that some CPLDs have over FPGAs is the programmable, T-type register. For some state-machine designs, such devices can significantly reduce the amount of required logic, producing a compact and fast implementation. Counters implemented in CPLDs using T-type registers usually use fewer product terms than those implemented in CPLDs that use D-type registers. As the width of the counter increases, the number of product terms saved also increases. Furthermore, the addition of features such as load, enable, reset, and preset does not add significant logic requirements, and you can implement these features at the maximum rated frequency of the device. However, vendors of some CPLD families rate the maximum performance of a device differently for T- and D-type devices (**Ref 1**).

When targeting a state-machine application into an FPGA, choose a state-encoding technique that minimizes the logic between each state transition. One example of this type of state encoding is called "one-hot" state encoding, which uses one register per state. Thus, a one-hot-encoded state machine with 12 states would require 12 registers. Such a machine can take advantage of the more register-intensive architecture of an FPGA. The ultimate goal is to reduce the state-transition logic to a single logic cell.

Just like in CPLDs, for simple state machines, one-hot encoding may be too simplistic and require more registers than an alternative approach that would employ fewer registers but more transition logic between each register. You would have to base this decision on the synthesis-tool and place-and-route results.

When deciding between an FPGA and a CPLD for a state-machine application, consider the performance requirements along with the logic complexity required for each state transition. CPLDs are inherently faster than FPGAs in state-machine applications, as PREP benchmarks 3 and 4 show (**Table 1**). However, if performance is not the overriding concern, base your choice on state transition-logic requirements. Furthermore, other functions the application requires might weigh the decision in favor of an FPGA or a

DESIGN-TOOL CONSIDERATIONS

The decision on which design tool to use to describe, synthesize, and optimize a PLD design is as important as your selection of a PLD device. Frequently, an architecture might appear to have the appropriate resources for solving a design problem, but the actual result may fall short of your goal because the tool did not efficiently use those resources.

In selecting a tool, you can use a tool from the PLD vendor and tailored for the vendor's products or a tool from a third-party tool vendor. PLD vendors' tools support a given architecture, so they can perform architecture-specific synthesis at the front end and are usually more efficient than are third-party tools. PLD vendors deliver more efficient optimization and mapping capability earlier than do third-party tool vendors. Third-party vendors must serve a broad range of users, and survival does not depend on supporting one vendor.

On the other hand, you may already have a design environment built around a third-party vendor's tools and want to incorporate PLD design into your design process. You may also prefer a tool that supports a broad range of PLDs so you don't have to learn a new tool every time you use a different vendor's devices.

In the short term, a PLD vendor's tool can get you started easily, provide good optimization and mapping for the target architecture, and is usually low-cost. Some PLD vendors' tools support a wide range of devices. For example, Cypress's Warp3 tools support PLDs, complex PLDs (CPLDs), and field-programmable gate arrays (FPGAs). In the long term, the ongoing integration of PLD vendors' synthesis and place-and-route engines into third-party tools will continue to improve the tools' efficiency and effectiveness.

CPLDs historically have been more amenable to traditional third-party approaches that generally synthesize a product's logic into a standard format. Getting a tool to map to the widely varying FPGA architectures requires different synthesis and optimization strategies. The ultimate consideration may be one of design style: whether to use a hardware-description language, such as VHDL, or a schematic-capture approach. The schematic-capture approach lets you tailor your design to the idiosyncrasies of an architecture. This typically library-based design, and some tools even provide users with a VHDL-based version of the library components.

However, using VHDL or another HDL lets you quickly run your design through one or more tools to see how they map to the target device. Doing your own benchmarking of various synthesis tools is a good idea. Programmable Electronics Performance Corp (PREP) is considering undertaking such an activity, which should users should support.

The PREP benchmarks are useful as rough performance and capacity indicators, but be aware of their limitations. You might interpret the benchmark results to indicate that one device gets twice as many instances as any other in building a state machine. But the tool you use or the design style you employ may not give you the same level of efficiency. The synthesis to the target device affects the resulting design. It is, therefore, important to understand what kind of special or architecture-specific synthesis and optimization techniques are available in the tool to get the most efficient design.

CPLD. Alternatively, you could explore both FPGA and CPLD options after synthesis and place-and-route and base your decision on actual simulated performance in the application. In this case, choose state-encoding methods separately for each target architecture to take advantage of the device's inherent architectural characteristics.

Arithmetic functions

In general, FPGA architectures are more adaptable to arithmetic applications than are CPLD architectures. The simplest type of arithmetic application is an accumulator. The 16-bit accumulator circuit is one of the PREP benchmarks, and you can take advantage of the PREP benchmark data when deciding which type of architecture to use. Using the official PREP benchmark numbers, according to PREP PLD Benchmark Suite 1, Versions 1.2 and 1.3 for Benchmark 6, you can average the internal frequency for all the certified CPLDs. Then, average the same parameter for all of the certified FPGAs. (PREP does not endorse the averaging of PREP benchmarks.) Comparing these values shows that, for the accumulator circuit, FPGAs typically operate faster than do CPLDs.

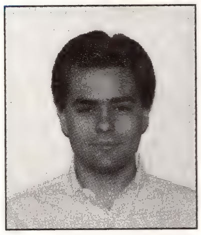
Most FPGAs have a much finer-grained architecture than that of CPLDs. The granularity also varies even among FPGA devices. The finer the grain of an architecture, the more flexibility it offers in implementing the logic associated with arithmetic circuitry. For example, the Cypress pASIC380 FPGA devices employ a multiplexer-based, logic-cell architecture that allows the implementation of efficient carry-select accumulator circuits. FPGAs that are not multiplexer-based excel in arithmetic applications because of dedicated carry calculation and passing circuitry built into the devices themselves.

Whatever your application, try many target architectures before choosing the device to use. This approach can be time-consuming and costly, however. Intelligently using the PREP benchmarks helps make your job easier and more satisfying. EDN

TABLE 1—CPLDs VS FPGAs IN PREP BENCHMARKS 3, 4, AND 6

Device	Internal frequency	BM3	BM4	BM6
CPLDs	Altera EPM7032-6	152	70	51
	Altera EPM7064-7	125	78	43
	Altera EPM7096-7	125	78	43
	Altera EPM7128-10	100	59	32
	Altera EPM7160E-10	100	63	32
	Altera EPM7192-12	91	53	31
	Altera EPM7256E-12	91	53	31
	AMD MACH230-15	67	33	22
	Cypress CY7C371-143	143	87	50
	Cypress CY7C374-100	100	56	39
	Cypress CY7C375-100	100	45	39
	Lattice pLSI1048-80	78	43	30
	Lattice pLSI2032-135	135	61	19
	Xilinx XC7272A-16	62	62	32
	Xilinx XC73108-10	62	62	42
Average CPLD performance		102.07	60.93	35.73
FPGAs	Actel A1225-1	34	21	24
	Actel A1240A-2	39	24	29
	Actel A1280-1	29	17	21
	Actel A1425	46	28	36
	Actel A1240	29	18	22
	Altera EPF81188-2	45	17	59
	Altera EPF8282-2	49	20	60
	Altera EPF8452-2	45	17	58
	Altera EPF8820-2	45	18	57
	Altera EPF81500-2	41	18	57
	Altera EPF81500-2	41	18	57
	AT&T AT&T1C07-2	30	18	50
	AT&T AT&T1C07-3	38	22	62
	Quicklogic QL12X16-2	57	33	39
	Quicklogic QL8X12A-3	62	38	45
Average FPGA performance		43.07	22.80	43.87

Author's biography



Richard Kapusta is PLD software applications manager at Cypress Semiconductor (San Jose, CA), where he has worked for three years. At Cypress, he's engaged in product planning and working with third-party tool vendors and customers. He holds a BS in computer engineering from the University of Illinois, Urbana/Champaign. He enjoys skiing and music.

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Reference

1. Jones, Christopher, "Knowing your CPLD maximizes its resources," *EDN*, Jan 5, 1995, pg 117.

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CIRCLE NO. 157

THE ART OF THE SMALL

Precision capacitors for small spaces and a broad range of applications

The growing demand for smaller end products calls for fresh, challenging designs. Now, TOKIN is meeting this challenge with a newly expanded lineup of compact capacitors that makes it easier than ever to satisfy exacting miniaturization needs.

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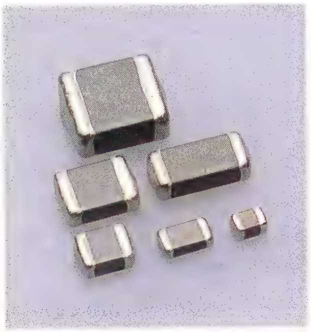
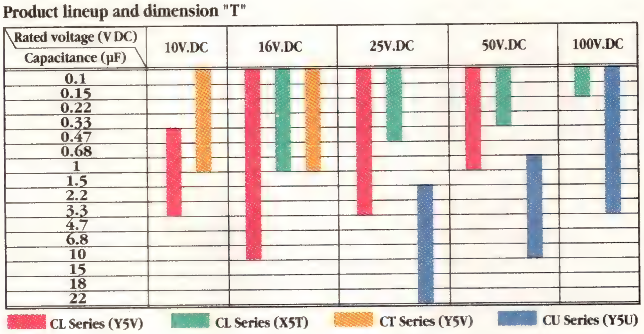
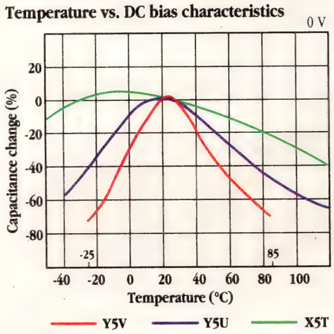


Product lineup and dimension "T"



Temperature vs. DC bias characteristics



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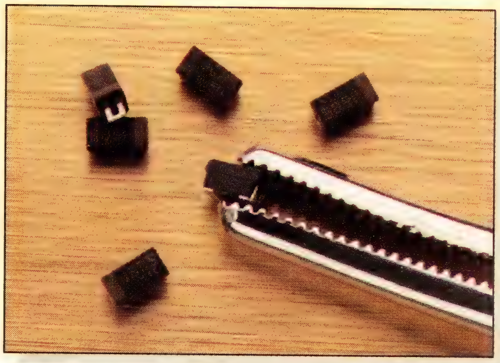
CIRCLE NO. 66

COMPONENTS SHOWCASE

- RESISTORS
- CAPACITORS
- INDUCTORS



TANTALUM CHIP CAPACITOR WITH FUSE.

The TCF Series of tantalum chip capacitors includes a built-in fuse to protect against the possibility of fire if the polarized device is mounted incorrectly. The capacitors are available in values from 1 to 10 μF in the A (3216) case size and up to 33 μF in the B (3528) case size. Rated voltages range from 4 to 35V. Tests on the TCF devices after soldering show 4Ω equivalent series resistance. Prices range from \$0.085 to \$0.105 (1,000,000). **Rohm Corp, Electronics Div,** Nashville, TN. (615) 641-2020. **Circle No. 425**

LINE-MATCHING TRANSFORMER FITS PCMCIA CARDS.

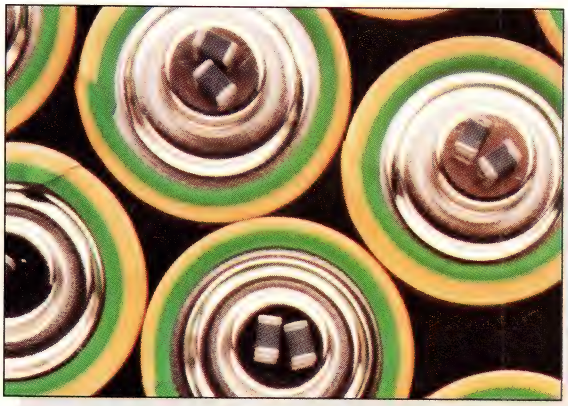
The PT73086 surface-mount line-matching transformer has a maximum height of 0.172 in. and a footprint of 0.790×0.670 in. The device meets the V.32 and V.32bis standards for modem applications. Key specifications include a nominal impedance of 600Ω, –76-dB distortion, and an insertion loss of 3.15 dB at 1 kHz. The device costs \$1.05 (100,000). **Datatronics Inc,** Romoland, CA. (909) 928-7700.

Circle No. 426

LOW-PROFILE TANTALUM CHIP CAPACITOR.

The Type 592D tantalum chip capacitor measures 0.047 in. above the board. The conformally coated device fits standard molded chip-mounting-pad dimensions. The 12 capacitance values are available from 1.0 to 100 μF with voltage ranges from 4 to 35V at 85°C. Typical performance ratings for a 22-μF, 16V dc device at 25°C include an ESR of 1.85Ω at 100 kHz, a dc-leakage current of 0.01 μA/CV, and a dissipation factor of 6% at 120 Hz. Typical price for a 10-μF capacitor with a 10W-Vdc rating and a ±20% tolerance is \$0.336 (1000). **Sprague,** Columbus, NE. (402) 563-6350.

Circle No. 427



SURFACE-MOUNT CHIPS SUPPRESS EMI.

The LCB-0805 EMI suppressor has a standard 0805 footprint, 600Ω impedance, and a dc resistance of 1.0Ω. The JCB-0805 has a 300Ω impedance and a dc resistance of 0.5Ω. The KCB-0805 has a 120Ω impedance and a dc resistance of 0.6Ω. Maximum current for all devices is 200 mA. Operating temperatures are from –55 to +125°C. The devices cost \$0.11 (100,000). **Associated Components Technology,** Garden Grove, CA. (714) 636-2645.

Circle No. 428

(continued on pg 120)

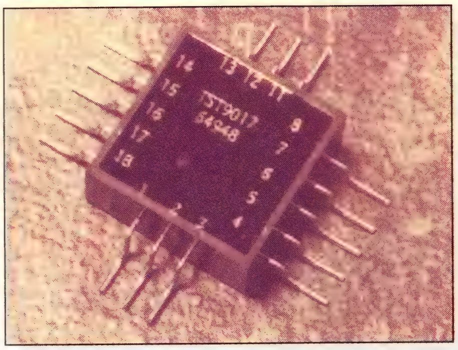
SHOWCASE COMPONENTS

- RESISTORS
- CAPACITORS
- INDUCTORS

ISOLATION TRANSFORMERS.

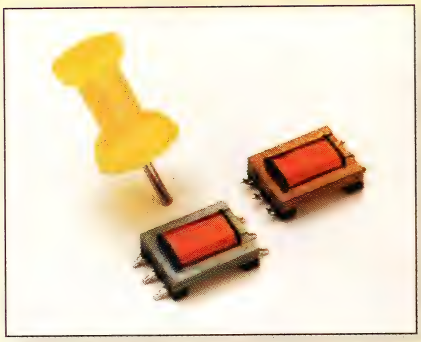
DU and SU series isolation transformers accommodate international input voltages and are available in models from 250 VA to 10 kVA, with the VA rating doubled for autotransformer connections. The transformers feature 2500V-rms HIPOT, Class A insulation (105°C) and a grounded 2-mil-thick copper-foil electrostatic shield. They are designed with dual primaries (DU Series) and secondaries (SU Series). Windings are identically rated at 0/104/110/120V ac or 0/208/220/240V ac, letting you

connect primary and secondary windings in series or in parallel. Prices range from \$53.50 to \$480 (100). **Signal Transformer Company Inc,** Inwood, NY. (516) 239-5777. **Circle No. 429**



DUAL MIL-STD-1553 TRANSFORMER HAS SMALL FOOTPRINT.

The TST-9000 has a case measuring 0.625×0.625×0.28 in. high. The dual transformer has a 10,000-hr life expectancy and meets the MIL-STD-1553 requirements for component isolation and common-mode rejection ratio. The transformers are encapsulated in a diallyl phthalate case and tested in compliance with MIL-T-21038 and MIL-STD-202. All models have center-tapped primaries and multi-tapped secondaries to accommodate existing systems. The transformers cost \$90 (10). **Beta Transformer Technology Corp,** Bohemia, NY. (516) 244-7393. **Circle No. 430**



SURFACE-MOUNT TRANSFORMERS FOR PCMCIA MODEM APPLICATIONS.

The transformers meet the voice, data, and facsimile requirements of the V.34bis 28,800-bps protocol. The transformer-mounting footprint measures 0.33×0.40 in., and the height measures 0.164 in. It has a turn ratio of 1:1 and a frequency response of 0.15 to 0.35 dB from 300 to 3500 Hz. Insertion loss is 2.7 dB ±0.4 dB, and return loss is 25 dB minimum at 300 to 3500 Hz. Total harmonic distortion is 82 dB typical and 89 dB maximum at 600 Hz and –10 dBm. These transformers meet the telecommunications requirements of FCC Part 68. The TTC-103SL is for surface mounting with board cutout; the TTC-203SL is for surface mount; and the TTC-303SL has a through-hole mounting. The transformers cost \$3.52 (5000). **Tamura Corp of America,** Temecula, CA. (909) 699-1270. **Circle No. 431**

(continued on pg 123)

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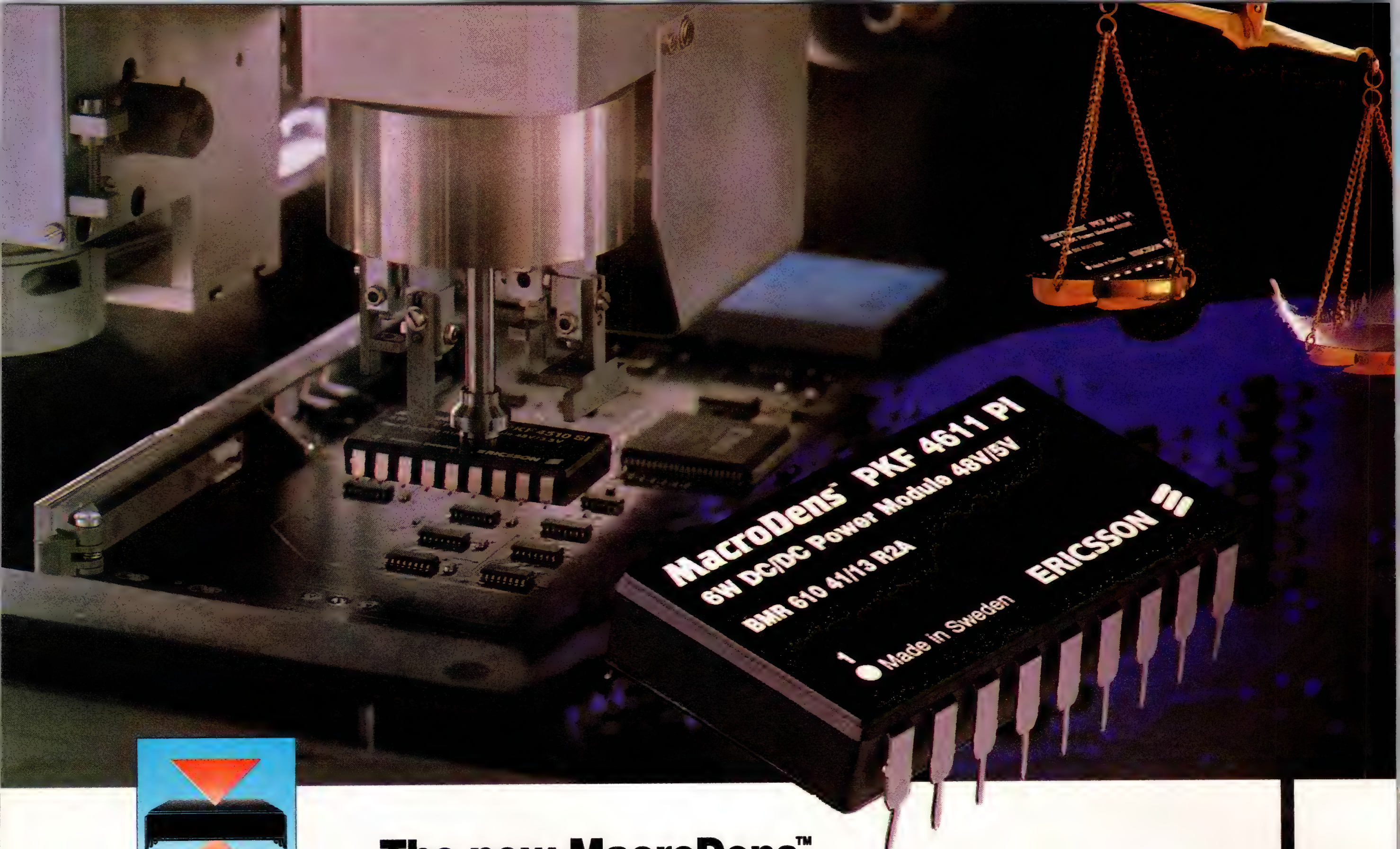

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ERICSSON

COMPONENTS SHOWCASE

- RESISTORS
- CAPACITORS
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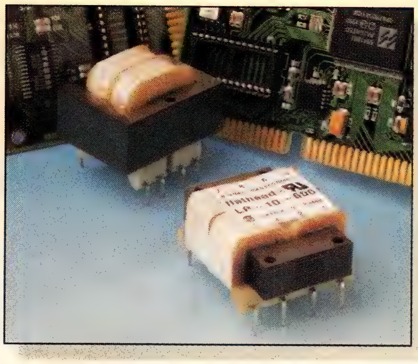
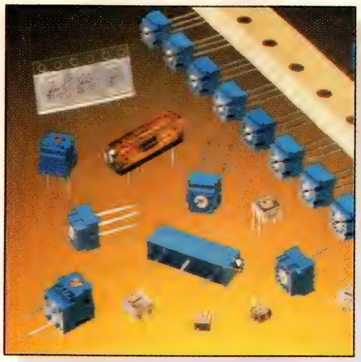


LOW-PROFILE TRANSFORMERS HAVE HEIGHTS RANGING FROM 0.65 TO 1.375 IN.

Flathead low-profile transformers operate in the 2- to 48-VA range. The transformers feature 1500V rms HIPOT, Class B insulation (130°C), dual primaries (115/230V at 50/60 Hz), and series or parallel secondaries. They use semitoroidal construction to minimize radiated magnetic fields. Split-bobbin construction eliminates the need for an electrostatic shield. The transformers are recognized to UL 506, and they are CSA certified to C22.2. Prices range from $5.08 to $9.68 (100). **Signal Transformer Co Inc,** Inwood, NY. (516) 239-5777.
Circle No. 432

SEALED CERMET TRIMMING POTENTIOMETERS.

The TR Series trimming potentiometers are sealed to withstand automated soldering and cleaning processes. The cermet resistive elements provide setting accuracy and



stability over a wide temperature range. Single-turn surface-mount models include the TR03 (3 mm square) and TR04 (4 mm square). In addition, 15 through-hole models are available with versions having single-turn, double-turn, and 12-turn operation. Resistance values range from 10Ω to 2 MΩ. Prices start at $0.39 (1000). **C&K Components Inc,** Watertown, MA. (617) 926-6400. **Circle No. 433**

POWER TOROIDAL INDUCTOR FOR DC/DC CONVERTERS.

The LPT-4545 provides high efficiency and low EMI radiation for dc/dc converter applications. The inductor has two separate windings, letting you connect them in series for higher inductance or in parallel for low dc resistance. The standard series includes 14 values ranging from 10 to 1200 μH. Current ratings range to 4A. The case measures 0.45 in. in diameter and 0.25 in. high. Typical price for a 10-μH device with a 4A current rating is $2.20 (5000). **Dale Electronics Inc,** Yankton, SD. (605) 665-9301.
Circle No. 434

SNUBBER CAPACITORS FOR IGBT MODULES.

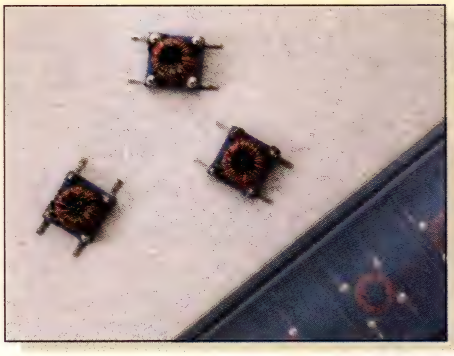
The PMB Series capacitors feature mounting lugs that attach directly to the terminals of IGBT modules. In addition to ease of mounting, the new design also provides higher reliability in vibration- or shock-prone applications. The capacitors are constructed in a rectangular-box package and are available in ranges from 0.1 to 2.5 μF and voltage ratings from 850 to 2000W Vdc. $3.50 (1000). **Illinois Capacitor Inc,** Lincolnwood, IL. (708) 675-1760. **Circle No. 435**

(continued on pg 124)

SHOWCASE

COMPONENTS

- RESISTORS
- CAPACITORS
- INDUCTORS

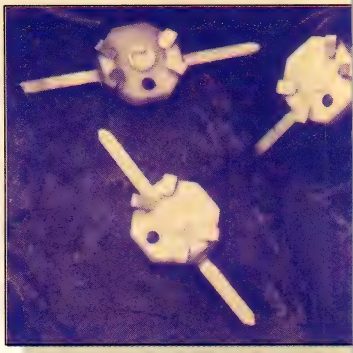


SURFACE-MOUNT TOROIDS.

KM Series toroids use molypermalloy powder cores, giving them a flat frequency response between 0 and 1 MHz. The toroids are designed for use as in-line noise filters in applications where the inductor must support 110 or 220V ac without core saturation. Inductances range from 10 to 250 μH, and dc resistance is between 0.04 and 0.7Ω. A 2A version can store 8 μJ, and a 0.25A version can store 20 μJ. The inductors have a 0.40×0.38-in. footprint and cost $1.60 (1000). **Associated Components Technology,** Garden Grove, CA. (714) 636-2645.
Circle No. 436

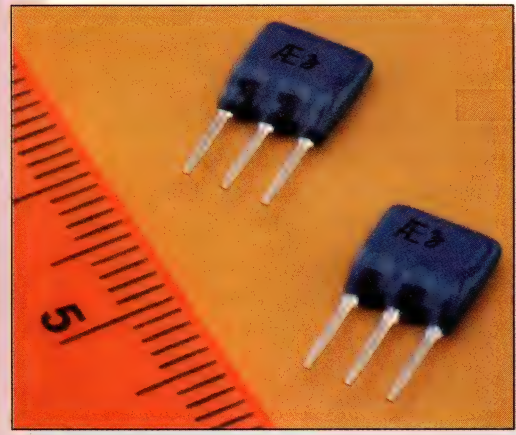
MAGNETIC MODULES FOR ATM 155-MBPS TRANSMISSION.

PE-6850X Series magnetic modules are designed for 155-Mbps transmission rates over data-grade unshielded-twisted-pair (UTP) copper wire. The new series also conforms to the proposed Fast Ethernet 100Base-TX standard and has been tested for interoperability with 100Base-TX hardware. The modules are designed to minimize the inherent problems of electromagnetic interference (EMI) and noise susceptibility encountered in 100/155-Mbit transmission over UTP cable. The modules provide 1500V rms isolation, wide bandwidth, and rise times of 2.5 nsec. Single-channel modules cost $3.28 (1000); dual-channel modules cost $4.32 (1000). **Pulse Engineering Inc,** San Diego, CA. (619) 674-8100.
Circle No. 437



2-GHZ MINIATURE TRIMMER CAPACITORS.

The Series 9401 Thin-Trim capacitors have a capacitance range of 0.25 to 0.7 pF through 1.5 to 4.0 pF and a Q>100 at 2 GHz. The trimmer capacitors have an operating temperature range of –55 to +125°C and are rated for 250V dc. Capacitor dimensions are 0.140 in. long×0.125 in. wide×0.040 in. high. They cost $1.02 (25,000). **Johanson Manufacturing Corp,** Boonton, NJ. (201) 334-2676.
Circle No. 438



TWO PRECISION RESISTORS IN THREE-TERMINAL NETWORK.

The SLD series resistor networks have a 0.25W power rating and values ranging from 50Ω to 30 kΩ. Absolute-resistance tolerances range from 0.05 to 1%; matching tolerances range from 0.02 to 1%. The resistors' temperature coefficient of resistance equals 0.4 ppm/°C with either ±2.5- or ±5-ppm tolerance. Temperature-coefficient tracking depends on the resistance ratio and ranges from ±0.5 ppm/°C to ±3 ppm/°C. A 1-kΩ/10-kΩ resistor combination with 0.4-ppm/°C ±5-ppm tolerance costs $4.15 (1000). **Isotek Corp,** Swansea, MA. (508) 673-2900.
Circle No. 439

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  Four Series / 18-380 VDC Input
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  True Redundancy Operation

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CIRCLE NO. 215

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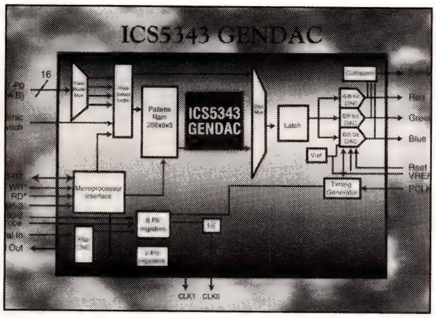
Memories for military and high-reliability applications offer SRAM, flash, and EEPROM versions. The family of 128k×32-bit memories is available in 68-pin J-lead packages. The EDI8C32128 SRAM is available with access times from 20 to 55 nsec. A low-power version provides data retention at 2V. The devices start at $652 (100). The EDI7C32128 flash memory comes with access times of 120 to 200 nsec; prices start at $652 (100). The EDI5C32128 EEPROM device offers 120- to 200-nsec access times and costs $2002 (1000). **Electronic Designs Inc**, Westborough, MA. (508) 366-5151. **Circle No. 328**



Integrated RAMDAC and programmable video-timing generator support 1600×1200-pixel resolution. The ICS5343 operates at pixel speeds to 170 MHz and supports a standard 16-bit pixel port that is compatible with most DRAM-based graphics controllers. The chip has a 256×six-color look-up-table palate RAM, a programmable-pixel clock-timing generator, and a programmable-memory clock-timing generator. The device comes in a 68-pin PLCC and costs $6.50 (10,000). **Integrated Circuit Systems Inc**, San Jose, CA. (408) 297-1201. **Circle No. 329**

PCMCIA controller chip for PCI bus supports two PCMCIA slots. The M5235 PCMCIA controller chip meets PCMCIA 2.1 and JEIDA 4.0 specifications. It works with 3.3 and 5V PC cards. The device comes in 208-pin TQFPs and PQFPs and costs $10.50. **Acer Laboratories Inc, Pacific Technology Group**, Santa Clara, CA. (408) 764-0644. **Circle No. 330**

Flash-memory cards have up to 20-Mbyte capacity. The D-Series flash-memory cards are PCMCIA Type I cards operating from a 5V supply. The cards have a low-power standby mode that requires <1 mA. Memory is organized into 64-kbyte sectors, each with a guaranteed minimum of 100,000 write\erase cycles. The 4-Mbyte AmC004-DFLKA costs $131 (1000), the 8-Mbyte AmC008DFLKA costs $219 (1000), and the 20-Mbyte Am020DFLKA costs $494 (1000). **Advanced Micro Devices Inc**, Sunnyvale, CA. (408) 749-5703. **Circle No. 331**

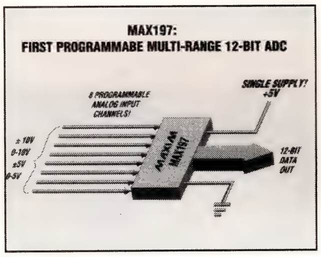
256k×16-bit DRAM has 50-nsec row-address-strobe access time and 22-nsec EDO page-mode cycle time. The 4-Mbit V53C16258H extended-data-out (EDO) suits applica-

tions such as graphics accelerators, set-top boxes, disk drives, laser printers, and communications buffers. The memory comes in a 40-pin SOJ package and costs $22 (10,000). **Mosel Vitelic**, San Jose, CA. (408) 433-6000. **Circle No. 332**

Dual-channel, 14-bit, correlated-double-sampling, CCD analog processor. The ET4265 provides 14-bit resolution at throughput rates to 2 MHz. The device has 0.3-LSB-rms noise, an 84-dB dynamic range, and a ±0.5 LSB differential nonlinearity. Power consumption is 2.8W for the 2.5×2.5×0.4-in. module. The ET4265 costs $694 (100), and the ET426501, with a digitally controlled dark-current offset, costs $796 (100). **Edge Technology Inc**, Waltham, MA. (617) 899-7900. **Circle No. 333**

4-Mbit flash memory available with 55-nsec access time. The Am29-F040 is organized as 512k×8 bits. The memory is divided into 64-kbyte sectors and is in-system programmable from a 5V supply. The device features the company's Embedded Program and Embedded Erase algorithms to simplify flash operations and free the host CPU from dedicated control of the device. The company guarantees the device for a minimum of 100,000 program\erase cycles. Available in 32-pin TSOP, PLCC/LCC, and DIP packages, the device costs $18 (1000). **Advanced Micro Devices Inc**, Sunnyvale, CA. (408) 749-5703. **Circle No. 334**

64-kbit parallel EEPROM has access times down to 100 nsec. The M28C64 has a page-write feature that lets you latch 64 consecutive bytes into memory and then program all 64 locations in one 2-msec program cycle. Organized as an 8k×8-bit device, the memory has a write/erase endurance of at least 100,000 cycles. The device features standard JEDEC byte-wide pinouts and has a minimum data retention of 10 years. Operating from a single 5V supply, the device draws 30-mA current while active and 100 μA in standby mode. It is available in 28-pin DIP, TSOP, SO28, and 32-lead PLCC packages. It costs $3.80 (10,000). **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300. **Circle No. 335**



12-bit, 100k-sample/sec ADC has eight input channels with software-programmable ranges. The MAX197's eight input channels are independently software programmable to accept 0 to 5, 0 to 10, ±5, and ±10V signals. The device operates from a 5V supply and tolerates ±16.5V on any input channel without affecting the conversion results on other channels. The overvoltage tolerance makes the device suitable for interfacing to ±15V-powered sensors without additional circuit protection. A byte-wide digital output provides data in an 8+4-bit format. The converter includes a 5-MHz bandwidth track/hold amplifier. The device uses an internal 4.096V reference or an external reference. The device comes in a 28-pin DIP, SO, and SSOP packages, and prices start at $9.90 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 336**

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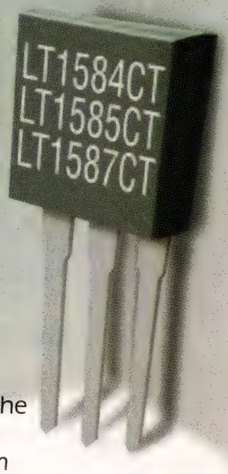

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CIRCLE NO. 11

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Video encoder converts RGB into luminance, chrominance, and composite video. The AD722 video encoder generates National TV Systems Committee or phase-alternation-line standard video from red, green, and blue color-component signals. The device's composite- and S-video outputs have a typical differential gain of 0.1% and a typical differential phase of 0.1°. The device accepts a frequency subcarrier (FSC) or a 4FSC clock. When a clock is not available, the chip's internal oscillator and an external FSC crystal can create the FSC. The device also accepts the FSC clock from an external video source providing phase-locking, as required in Genlock applications. Operating from a single 5V supply, the device drives 75Ω reverse-terminated loads. The 16-pin SOIC costs $3.55 (10,000). **Analog Devices Inc**, Wilmington, MA. (617) 937-1428.

Circle No. 337

High-speed coil drivers integrate logic, MOSFETs, and MOSFET drivers on single IC. The EL7240C and EL7241 coil driver ICs have a 20-nsec propagation delay and a 2A pk drive current. The drivers have a 3Ω output impedance and operate at 4.5 to 16V. They are compatible with 3 and 5V logic inputs. The devices operate as coil drivers for computer-tape-drive-backup systems, but they are also useful for other applications requiring high-speed and high-current drive capabilities. Prices for the devices start at $1.90 (1000). **Elantec Inc**, Milpitas, CA. (408) 945-1323.

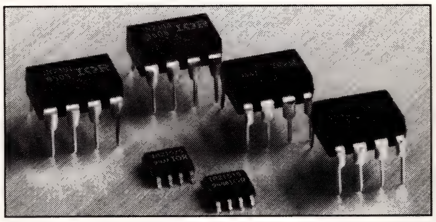
Circle No. 338

Two-port isolated amplifier has instrumentation amplifier inputs. The ISO213 is intended for applications with low signal levels needing galvanic isolation. It has a ±10 input-signal range, ±40V input-overvoltage protection, and a 0.5 to 5000 gain range. The device operates from a 12 to 15V supply and dissipates 45 mW. It is rated for continuous operation at 1500 or 2500V rms pulsed, and has nonlinearity specifications compatible with 12-bit conversion systems. The device comes in a low-profile, 38-pin ZIP package and costs $29.65 (100). **Burr-Brown Corp**, Tucson, AZ. (602) 746-1111.

Circle No. 339

Low-cost isolation amplifiers are rated for 500V-rms input isolation. The AD104 and AD102 use transformer-coupled galvanic isolation and have 100-dB common-mode rejection. The AD102 is a stand-alone device with 1.5-kHz, full-power bandwidth. It operates from a 15V supply and dissipates 75 mW. The AD104 for multichannel systems requiring input-to-input isolation has a 4-kHz bandwidth and requires a 25-kHz, 15V square-wave clock source. Both devices come in SIP-style packages measuring 2.08×0.26×0.625 in. The AD104 costs $20.55 (1000), and the AD102 costs $22 (1000). **Analog Devices Inc**, Wilmington, MA. (617) 937-1428.

Circle No. 340



Low-cost control ICs for driving power MOSFETs and insulated-gate bipolar transistors. A family of eight 600V control ICs for specific applications costs $1.20 for samples and $0.75 for production volumes. For motor control, the IR2101 provides a high- and low-side drive. The IR2102 also provides a high- and low-side drive with inverted inputs. For power supplies, the IR2103 provides a high- and low-side drive with dead time and one inverted input. The IR2104 half-bridge driver has dead time and shutdown. For single-channel driver applications not requiring both high- and low-side drives, the IR2117 has a noninverted input, and the IR2118 has an inverted input. For electronic ballast, the IR2151 provides a self-oscillating half-bridge driver, and the IR2152 provides a self-oscillating half-bridge driver with inverted output phase. **International Rectifier Corp**, El Segundo, CA. (310) 322-3331. **Circle No. 341**

Power-supply chip for switching power supplies of >1000W. The ML4822 first-stage power-factor-correction chip converts ac-line voltages of 85 to 265V into a steady 400V regulated output with a power factor >0.99. The chip uses an active snubbing cir-

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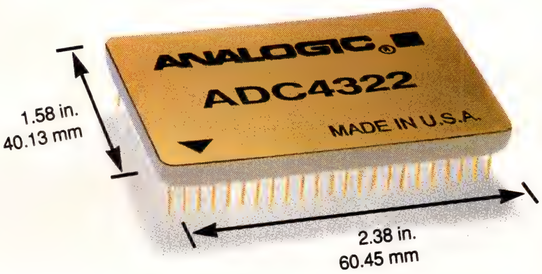

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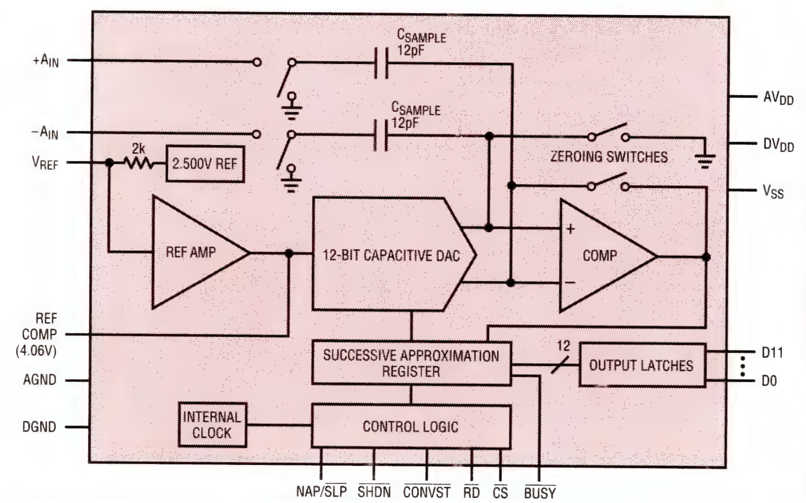
CIRCLE NO. 212

LINEAR TECHNOLOGY

Linear Solutions
Data Conversion

LTC1410 Breaks 12-Bit, 1Msps Barrier with 71dB SINAD at Nyquist!

New LTC1410 12-Bit, 1.25Msps ADC



The LTC1410 is a 12-bit, 1.25Msps, sampling ADC designed for demanding telecom and signal analysis applications. It delivers true 12-bit performance from DC to Nyquist at unprecedented low cost and power dissipation.

Key features are:
- 1.25Msps throughput
- 71dB S/(N+D) at Nyquist
- 160mW typical power dissipation, 12mW nap mode, 100µW sleep mode
- Complete, sampling ADC
- True differential inputs reject common-mode noise

The LTC1410 contains a wideband sample-and-hold, precision voltage reference and high speed, parallel interface to DSP and microprocessor ports. Two digitally selectable power-down modes allow optimal power saving and response time for low power systems. A unique differential input can acquire single-ended or differential signals while rejecting wideband, common-mode noise. Packaged in 28-pin SO the LTC1410 is available screened to the commercial and extended industrial temperature ranges. Pricing begins at $23.00 in 1000-piece quantities.

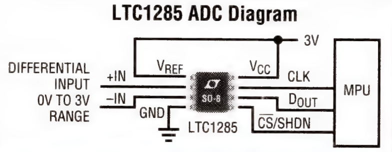
Circle No. 102: Please send literature. Circle No. 103: Call me. I'm interested.

Tiny 3V, 12-Bit ADCs Draw 160µA and Shut Down to 1nA

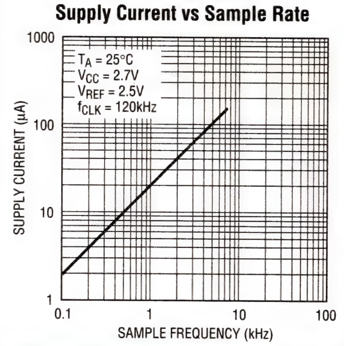
The LTC1285/LTC1288 are tiny 12-bit ADCs designed to operate on 3V supplies. They draw only 160µA of supply current and automatically power down to 1nA between conversions. Packaged in 8-pin DIP and SO the LTC1285/LTC1288 pricing begins at $6.22 in 1000s, perfect for space and power sensitive applications such as pen screen interface, remote data acquisition and battery monitoring.

The LTC1285 features a differential input while the LTC1288 input is 2-channel multiplexed. Both devices have 3-wire serial I/O compatible with the SPI and Microwire™ interface standards and easily accommodate isolated applications. The LTC1285 is offered screened to the extended industrial temperature range.

LTC1285 ADC Diagram



LTC1285/LTC1288
Supply Current vs Sample Rate

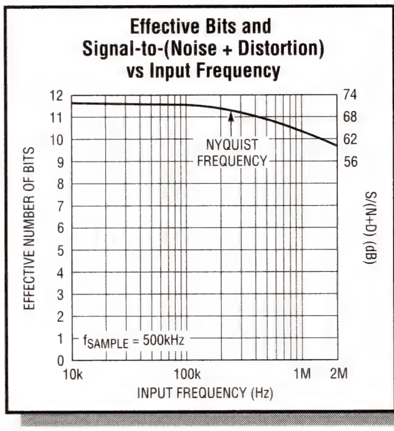


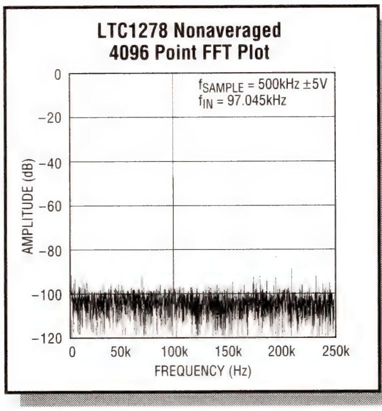
Circle No. 104: Please send literature. Circle No. 105: Call me. I'm interested.

Complete 12-Bit ADC Operates on Single 5V Supply at 500KSPS

The LTC1278 is a 12-bit, 500ksps ADC perfect for demanding low power applications such as telecom, vibration analysis and portable DSP.

Outstanding performance includes:
- 400ksps (LTC1278-4) and 500ksps (LTC1278-5) throughput
- 70dB S/(N+D) at Nyquist
- 75mW power dissipation and 8.5mW power shutdown
- Complete ADC in small footprint
- Single 5V or ±5V supply



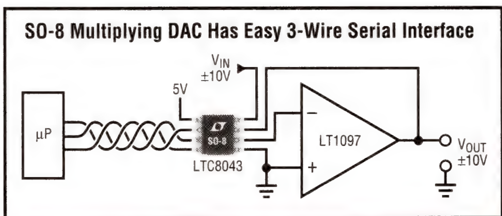


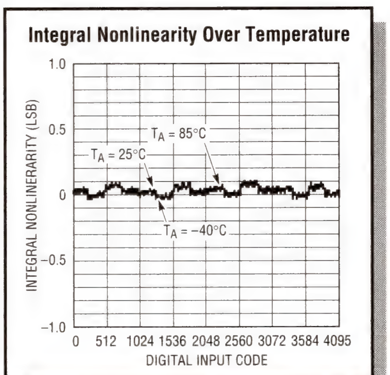
The LTC1278 contains a sample-and-hold, synchronized conversion clock, precision voltage reference and high speed, parallel interface to DSP and microprocessor ports. The ADC features a 8.5mW power-down mode with instant wake-up for maximizing power savings. Input range is 0V to 5V on a single 5V supply and ±2.5V with ±5V supplies. For applications requiring additional throughput the LTC1279 provides a pin compatible 600ksps ADC. Pricing begins at $12.00 in 1000-piece quantities.

Circle No. 106: Please send literature. Circle No. 107: Call me. I'm interested.

Serial 4-Quadrant Multiplying 12-Bit DAC Available in SO-8

The LTC8043 is a serial input 12-bit multiplying DAC that is a superior pin compatible replacement for the DAC-8043. Improvements include better accuracy, better stability over temperature and supply variations, lower sensitivity to output amplifier offset, tighter timing specifications and lower output capacitance.



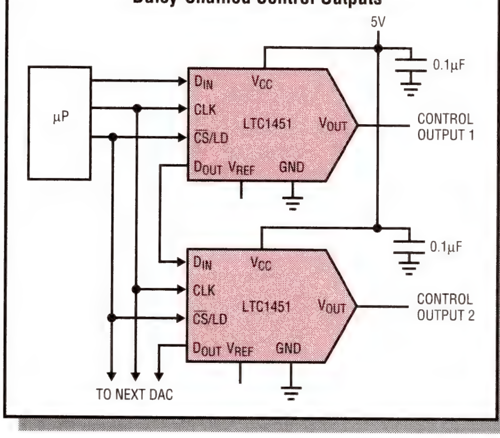


Outstanding specifications include :
- Maximum DNL and INL over temperature ±0.5LSB
- ± 1LSB maximum gain error
- 5 ppm/°C maximum gain temperature coefficient
- Total Harmonic Distortion (THD): 108dB typical

The LTC8043 is extremely versatile. It can be used in a variety of 2- and 4-quadrant applications such as: programmable gain amps, digitally controlled filters and power supplies, process control and industrial automation. Packaged in 8-pin DIP or SO, the LTC8043 is available screened to the extended industrial temperature range of −40°C to 85°C. Pricing begins at $4.80 in 1000s.

Circle No. 108: Please send literature. Circle No. 109: Call me. I'm interested.

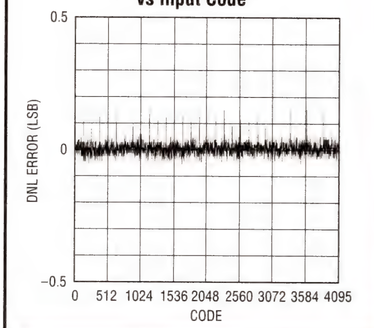
Complete Voltage Output 12-Bit DACs Have Rail-to-Rail Swing in SO-8



Daisy-Chained Control Outputs

The LTC1451/LTC1452/LTC1453 are micropower rail-to-rail voltage output 12-bit DACs in 8-pin DIP and SO. The devices have an easy-to-use, 3-wire serial interface that is cascadable, allowing multiple DACs on a single data I/O line.

Key features are:
- Single 3V or 5V supply
- Built-in reference: 2.048V (LTC1451), 1.220V (LTC1453)
- Multiplying version: LTC1452
- Power-on reset
- Maximum DNL < ±0.5LSB



Differential Nonlinearity vs Input Code

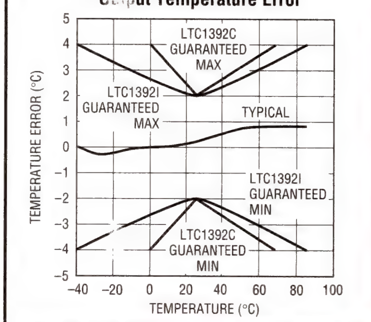
The devices dissipate only 2mW on 5V supply and 750µW from 3V, making them ideal for low power designs including: cellular telephony, POS systems, industrial process controls, wireless communications and general trim-pot applications. The output range includes both rails with improved capacitive load handling capability over competing solutions. Available screened to the commercial and industrial temperature ranges. Pricing begins at $4.20 in 1000-piece quantities.

Circle No. 110: Please send literature. Circle No. 111: Call me. I'm interested.

Unique, Data Acquisition Device Provides a Variety of Environmental Monitoring Functions

The LTC1392 is a micropower, 10-bit data acquisition system designed to measure ambient temperature, on-chip supply voltage and differential common-mode rail-to-rail input signals. The device accomplishes these functions in a single SO-8 package and dissipates less then 2.5mW.

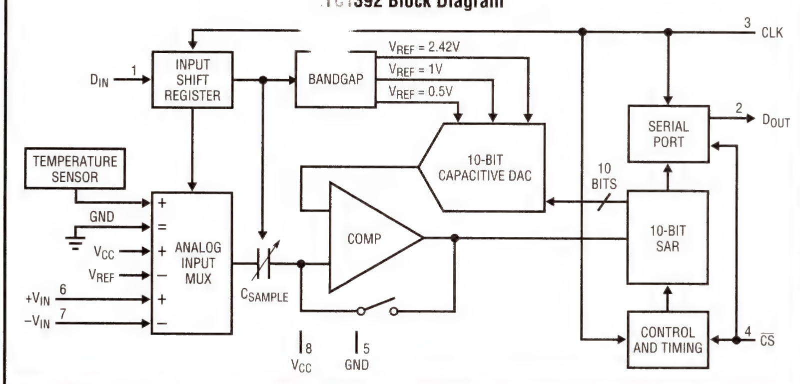
The LTC1392 features:
- 10-bit sampling ADC
- High accuracy bandgap reference
- 3-wire half-duplex serial interface
- On-chip temperature sensor
- A 3-channel multiplexer
- Rail-to-rail common-mode input



LTC1392 Output Temperature Error

The LTC1392 is suited for a wide variety of environmental monitoring applications including: power distribution systems, temperature measurement, airflow, relative humidity, pressure and weight measurement.

LTC1392 Block Diagram



The LTC1392 is available screened to the commercial and industrial temperature ranges. Pricing begins at $3.94 in 1000-piece quantities.

Circle No. 112: Please send literature. Circle No. 113: Call me. I'm interested.

Sampling A/D Converters

Part	Resolution (Bits)	F_{SAMPLE} (ksps Max)	# of Inputs	V_{REF}	Data* I/O	V_{CC} (V)	P_{DISS}** (mW)	Features	Package†
LTC1096	8	33	1	Ext	Serial	2.7-9	0.6/0	Micropower SO-8 ADC	N8/S8
LTC1098	8	33	2	Ext	Serial	2.7-6	0.6/0	2-Channel LTC1096	N8/S8
LTC1196	8	1000	1	Ext	Serial	2.7-6	55	1Msps SO-8 ADC	N8/S8
LTC1198	8	750	2	Ext	Serial	2.7-6	55/0	2-Channel LTC1196	N8/S8
LTC1090	10	30	8	Ext	Serial	4-9	5	Low Power Multiplexed ADC	N20/S20
LTC1091	10	31	2	Ext	Serial	4-9	7.5	8-Pin 2-Channel ADC	N8
LTC1092	10	38	1	Ext	Serial	4-9	5	8-Pin 10-Bit ADC	N8
LTC1093	10	26	6	Ext	Serial	4-9	5	Low Power Multiplexed ADC	N16/S16
LTC1094	10	26	8	Ext	Serial	4-9	5	Low Power Multiplexed ADC	N20
LTC1095	10	26	6	+5.0	Serial	4-9	15	Complete 6-Channel ADC	N18
LTC1283	10	15	8	Ext	Serial	3-3.6	0.45	3V LTC1090	N20
LTC1285	12	7.5	1	Ext	Serial	2.7-6	0.48/0	3V LTC1286	N8/S8
LTC1286	12	12.5	1	Ext	Serial	4-9	1.25/0	Micropower SO-8 12-Bit ADC	N8/S8
LTC1288	12	6.6	2	Ext	Serial	2.7-6	0.63/0	3V LTC1298	N8/S8
LTC1298	12	11.1	2	Ext	Serial	4-6	1.25/0	2-Channel LTC1286	N8/S8
LTC1290	12	50	8	Ext	Serial	4-6	30/0.05	8-Channel ADC	N20/S20
LTC1291	12	54	2	Ext	Serial	4-6	30/0.05	8-Pin 2-Channel ADC	N8
LTC1292	12	60	1	Ext	Serial	4-6	30	8-Pin 12-Bit ADC	N8
LTC1293	12	46	6	Ext	Serial	4-6	30/0.05	6-Channel ADC	N16
LTC1294	12	46	8	Ext	Serial	4-6	30/0.05	8-Channel ADC	N20/S20
LTC1296	12	46	8	Ext	Serial	4-6	30/0.05	LTC1294 w/Shutdown Output	N20/S20
LTC1297	12	50	1	Ext	Serial	4-6	30/0.05	LTC1292 w/Auto-Shutdown	N8
LTC1287	12	30	1	Ext	Serial	2.7-6	3	3V LTC1292	N8
LTC1289	12	25	8	Ext	Serial	2.7-6	3/0.03	3V LTC1290	N20/S20
LTC1272-8	12	100	1	2.42	µP 8 or 12	+5	75	Sampling AD7572-12	N24/S24
LTC1272-3	12	250	1	2.42	µP 8 or 12	+5	75	Sampling AD7572 A-3	N24/S24
LTC1273	12	300	1	2.42	µP 8 or 12	+5	75	5V High Speed ADC w/Ref	N24/S24
LTC1274	12	150	1	2.42	12	5/±5	15/0.005	Low Power Sampling ADC w/Shutdown	S24
LTC1275	12	300	1	2.42	µP 8 or 12	±5	75	High Speed ADC w/Ref	N24/S24
LTC1276	12	300	1	2.42	µP 8 or 12	±5	75	High Speed ADC w/Ref	N24/S24
LTC1277	12	150	1	2.42	µP 8	5/±5	15/0.005	Low Power Sampling ADC w/Shutdown	S24
LTC1278-4	12	400	1	2.42	µP 12	3/±3	75/5	Sampling ADC w/Shutdown	N24/S24
LTC1278-5	12	500	1	2.42	µP 12	3/±3	75/5	Sampling ADC w/Shutdown	N24/S24
LTC1279	12	600	1	2.42	µP 12	3/±3	75/5	Sampling ADC w/Shutdown	N24/S24
LTC1282	12	140	1	1.20	µP 8 or 12	3/±3	12	3V Sampling ADC	N24/S24
LTC1410	12	1250	1	2.50	12	±5	160/0.01	Sampling ADC w/Shutdown	S28

* Serial I/O is Microwire, SPI and QSPI compatible
** Power dissipation is listed in the Active and Shutdown modes
† N8 = 8-pin DIP N16 = 16-pin DIP N18 = 18-pin DIP N20 = 20-pin DIP N24 = 24-pin DIP N28 = 28-pin DIP
S8 = 8-pin SOIC S16 = 16-pin SOIC S20 = 20-pin SOIC S24 = 24-pin SOIC S28 = 28-pin SOIC

D/A Converters

Part	Resolution (Bits)	Output Type	V_{REF}	Data I/O	V_{CC} (V)	P_{DISS} (mW)	Features	Package
LTC1257	12	V	Int	Serial	4.5-15	1.75	Single Supply V_{OUT} DAC	N8/S8
LTC1451	12	V	Int	Serial	4.5-6.0	2.0	5V Rail-to-Rail V_{OUT} DAC	N8/S8
LTC1452	12	V	Ext (MDAC)	Serial	3.0-6.0	1.12	Single Supply V_{OUT} MDAC	N8/S8
LTC1453	12	V	Int	Serial	3.0-4.5	0.750	3V Rail-to-Rail V_{OUT} DAC	N8/S8
LTC7541A	12	I	Ext (MDAC)	Parallel	5-16	15	Industry Standard MDAC	N18/S18
LTC7543	12	I	Ext (MDAC)	Serial	4.75-5.25	0.500	Industry Standard Serial MDAC	N16/S16
LTC8043	12	I	Ext (MDAC)	Serial	4.75-5.25	0.500	8-Pin SOIC MDAC	N8/S8
LTC8143	12	I	Ext (MDAC)	Serial	4.75-5.25	0.500	Industry Standard MDAC	N16/S16

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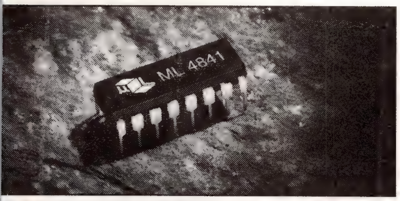
t to redirect power normally lost in tching back to the output, provid- ; efficiencies of 90 to 97%. The ice comes in a 16-pin DIP or SOIC ckage and costs $4.05. **Micro Linear rp**, San Jose, CA. (408) 433-5200.

Circle No. 342

ips for PCI-based multimedia plications. The IIT 3304 Multime- Encode Processor (MEP) single-chip ıltimedia authoring and playback ocessor lets you author and edit mul- iedia publications in real time. The p performs Moving Pictures Experts oup 1 video encoding and decoding ıs full-motion video capture. It nes in a 240-pin PQFP and costs $45 ,000). The IIT 3501 Video PCI Inter- e Chip connects all members of the mpany's Multimedia Processor chitecture family, including the MEP, ectly to the PCI bus. The device nes in a 160-pin PQFP and costs $18),000). **Integrated Information chnology Inc**, Santa Clara, CA. (408) 7-1885.

Circle No. 343



wer-supply chip uses two-stage nversion for power-factor cor- ction and conversion efficiency. e ML4841 accepts an ac input volt- e from 85 to 265V ac and converts it standard dc voltages, such as ±3.3 or V. The chip provides power-factor rection >0.99 and efficiencies >90%. e chip uses a two-stage conversion ocess. The first stage is optimized for high power-factor rating on the ac e, and the second stage is optimized high output efficiency. The chip ows power supplies to meet the C555 standard, which requires wer-factor correction for products er 50W sold in Europe in 1996. Avail- e in a 14-pin DIP or 16-pin SOIC ckage, the device costs $3.08 (1000). **cro Linear Corp**, San Jose, CA. (408) 3-5200.

Circle No. 344

deo line buffer operates at eeds to 50 MHz. The LF9501 has a ffer length programmable from 2 to 31 words to match line lengths of various video formats including National TV Systems Committee, phase-alternation-line, Systeme Electronique Couleur Avec Memoire, and other proprietary formats. The device accommodates a 10-bit word length. It comes in a 44-pin plastic J-lead chip carrier, and prices start at $13.23 (500). **Logic Devices Inc**, Sunnyvale, CA. (408) 737-3300.

Circle No. 345

MPEG 1 audio and video decoder chip. The CL480PC decodes Moving Pictures Experts Group (MPEG) 1 audio and video for portable and desktop computers. The chip features a host or CD interface for input of MPEG-1-system bit streams, the ability to load the microcode initializing the CL480PC via the host interface, 16-bit dithered video output; programmable output video timing and interpolation control, and advanced error concealment. The 128-pin PQFP dissipates <1W from a 3.3V supply while operating and <0.1W in stand-by mode. It costs $31 (OEM). **C-Cube Microsystems Inc**, Milpitas, CA. (408) 944-6300.

Circle No. 346

FIFO for printer applications. The GT-24002 PrintFIFO is a 32-bit-wide, 1104-location-deep, synchronous FIFO buffer. The device can output data 1 bit or 1 byte at a time. Input and output ports can operate at 33 MHz, providing an input bandwidth of 133 Mbytes/sec. The true dual-port device can simultaneously receive input data while outputting data. Additional features include margin counters and registers to support printer operations. The device comes in a 128-lead PQFP and costs $49.95 (5000). **Galileo Technology Inc**, San Jose, CA. (408) 451-1400.

Circle No. 347

LPGA has >100,000 gates and one-day delivery. The QYH600 family of laser-programmable gate arrays (LPGAs) offers densities of 17,000 to 120,000 available logic gates and supports system clock rates >120 MHz. The initial members of the family include 70,000- and 100,000-gate devices that will be available in the third quarter of 1995. Two tested 100,000-gate LPGAs with a five-day turnaround cost $70,000. **Chip Express Corp**, Santa Clara, CA. (408) 988-2445.

Circle No. 348

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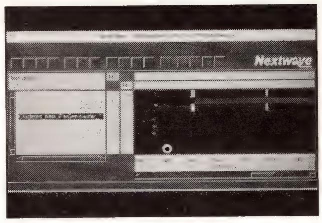
Design environment automates high-speed system-design methodology. The BoardQuest environment combines tools from the timing, signal-integrity, EMI, thermal, reliability, and manufacturing domains. The environment integrates with the company's Concept and Composer design-entry tools; the SigNoise, EMControl, Thermax, and Viable DesignFor analysis tools; and the Allegro correct-by-design layout system. Prices for BoardQuest start at $19,000. Prices for DesignFor analysis tools range from $18,000 to $35,000. **Cadence Design Systems Inc**, San Jose, CA. (408) 943-1234. **Circle No. 409**

Multilevel simulation tool for submicron designs. QuickVHDL Co-Lsim combines the QuickVHDL simulator with Lsim for transistor-level analysis of timing and power effects in deep-submicron designs. The co-simulation interface is based on the Precedence SimMatrix simulation backplane. A node-locked license costs $16,000, and a floating license costs $20,000. The tool requires Lsim and QuickVHDL. **Mentor Graphics**, Wilsonville, OR. (503) 685-8000. **Circle No. 410**

Graphical state-machine-design tool adds Verilog to supported languages. The StateCAD Verilog Edition translates bubble diagrams into synthesizable, Open Verilog International-compliant Verilog for tools from FrontLine, Simucad, and Exemplar. The tool also helps you analyze your state designs for problems. Other versions of StateCAD generate code in Abel, VHDL, and C from the same diagram. The Verilog edition costs $1495. **Visual Software Solutions**, Coral Springs, FL. (305) 346-8890. **Circle No. 411**



Tool links graphical timing and HDL specification to create Verilog testbenches. TesTech links the company's TDS, a graphical timing-specification tool, with its Visual HDL, a graphical hardware-descripti language- (HDL)-specif tion tool, to create Veri test benches. The t checks conformance of cuit timing to design spe cations throughout a desi It also simplifies stimu capture by using a stand data-book format to desc timing requirements. tool is available as an opt to TDS and Visual HDL costs $20,000. **Sum Design Inc**, Beaverton, (503) 643-9281. **Circle No.**

Tool combines static-t ing analysis and Veri spread-delay simulati The Epilog-MX multim timing-verification t checks the timing of all p of a design's logic in operation. Static-tim analysis quickly finds tim hazards for synchron

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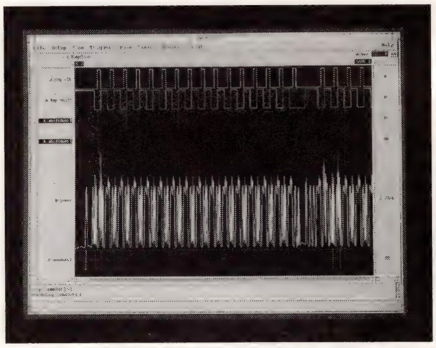
logic. The Verilog gate spread-delay simulation finds timing problems for nonsynchronous parts of a design. Although not as fast as static-timing analysis, the spread-delay simulation is necessary for some parts of most designs. Using the simulation for only those portions of a design in which static-timing analysis is inadequate saves time over a full timing simulation of the complete design. A single node-locked license costs $35,000. **Nextwave Design Automation**, San Jose, CA. (408) 437-3939.
Circle No. 413

PC-based semiconductor-device-simulation software. The Device Wizard simulates semiconductor devices on PCs. According to the company, the software's simulation speed and accuracy meets or exceeds that of Unix-based semiconductor-device simulators. The tool can simulate arbitrary 2-D semiconductor devices and includes predefined templates for >20 common semiconductor-device types. The base price is $12,000. **Dawn Technologies Inc**, Sunnyvale, CA. (408) 737-6181. **Circle No. 414**



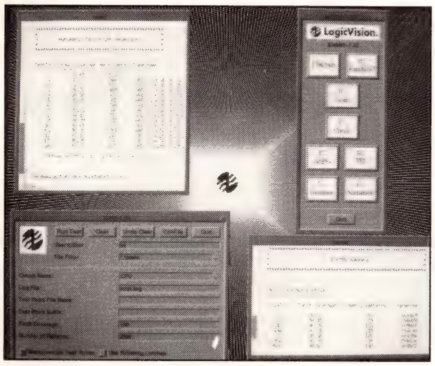
Power-calculation tool for ICs can handle bus-contention and state-dependent currents. PowerSim 2.0 performs power calculations on ICs described in Verilog HDL. It takes into account capacitive charging/discharging, slew effects, bus contention, state-dependent currents, leakage, and other power factors. According to the company, the tool operates at the cell level and runs at virtually the same speed as a gate-level simulation. The tool works with Verilog simulators and runs on SPARC, HP700, and DEC Alpha computers. It costs $18,500. **System Science Inc**, Palo Alto, CA. (415) 812-1800. **Circle No. 415**

PC-board-layout tool offers interface to Specctra autorouter. The WinBoard pc-board-layout tool now has an interface to the Specctra autorouter from Cooper & Chyan Technology. The interface lets you partially route a board before launching the autorouter and edit the board after autorouting. WinBoard PCB layout costs $995, and the interface costs $295. **Ivex Design International**, Beaverton, OR. (503) 531-3555.
Circle No. 416

New versions of analog and logic simulators. T-Spice version 3.0 improves computational efficiency, robustness, reliability, and accuracy over previous versions. A source-stepping feature adjusts power-supply values until it converges on the dc operat-

ing conditions. The tool also offers a lossy transmission-line model for modeling high-frequency effects, mismatch, and coupling between elements. Prices for the software for PCs and workstations start at $1245. Gate Sim version 2, a PC-based gate-level digital simulator, handles 250,000 gates and costs $1295. **Tanner Research Inc**, Pasadena, CA. (818) 792-3000. **Circle No. 417**

Spice library for power-supply designers. The Spice model library for power-supply designers contains >20 PWM IC models for parts from Cherry Semiconductor, Linear Technology, Siliconix, and Unitrode. Some models offer multiple levels of complexity. The models use Spice 3, Boolean-logic, and HDL elements. The model library works with the company's IsSpice3 or IsSpice4 simulators. It costs $395. **Intusoft**, San Pedro, CA. (310) 833-0710. **Circle No. 418**



BIST tool for ICs. ICBIST couples front-end generation of synthesizable register-transfer-level code for logic built-in self-test (BIST), RAM BIST, and Joint Test Action Group/1149.x with back-end tools for BIST analysis and testability insertion. The tool suits complex ASICs and custom ICs. Prices start at $140,000 per seat. **Logic Vision Software Inc**, San Jose, CA. (408) 453-0146. **Circle No. 419**

Windows-based EDA-design environment offers improvements. Workview Plus 5.2 offers a variety of improvements over earlier versions. The ViewDraw tool now supports bus rippers and net aliasing. ViewTrace includes faster database reads and refresh rates. The optimization engine for ViewFPGA includes direct mapping to field-programmable gate-array (FPGA) logic modules, mapping to complex I/Os, and links to macro generators. The new release costs $5000 to $45,000. **Viewlogic Systems Inc**, Marlborough, MA. (508) 480-0881. **Circle No. 420**

Verilog simulator now runs under Windows and OS/2. VeriWell 2.0 now is available for Windows, Windows NT, Windows 95, and OS/2. According to the company, the simulator complies with Open Verilog International standards and offers Verilog XL compatibility and performance. The base module costs $1495, the gates and timing-preference module cost $895, and both modules together cost $2390. **Wellspring Solutions Inc**, Sutton, MA. (508) 865-7271. **Circle No. 421**

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Real-time executive for component-based real-time executive. The MQX version 2.31 real-time executive has a minimum size of 8 kbytes for a Motorola 68000 processor and a maximum size of about 23 kbytes if using all 15 components. The executive includes a component if an application references the component. The actual size of the kernel is determined at link time. The new release gives you better control over the size and functionality of the executive. It costs $5000 on a per-project basis with a royalty-free source-code license. **Precise Software Technologies Inc**, Nepean, ON, Canada. (613) 596-2251, ext 27. **Circle No. 397**

PC/104 computers feature flat-panel displays. The DisplayPac-104 is available with 14-, 10.4-, and 8.4-in., VGA, color, thin-film-transistor (TFT) LCDs with up to 256,000 colors; 11.8-in., XGA, color TFT LCDs; dual-scan, passive-color LCDs; active-matrix, monochrome LCDs; electroluminescent displays; and monochrome LCDs. A complete system with a display, a 486 computer, a touchscreen, and a PC/104 expansion module is 2.5 in. thick. A 50-MHz system, including a touchscreen and 4 Mbytes of DRAM, costs $3782 (50). **Computer Dynamics**, Greer, SC. (803) 877-8700. **Circle No. 398**

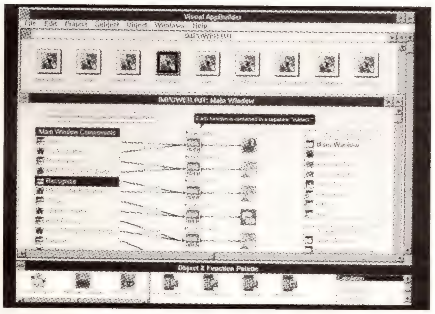
Tool lets you create and maintain graphical data models of PowerBuilder databases. Database Engineer for PowerBuilder lets you visually define systems for design specifications, documentation, and maintenance. The tool works with EasyCASE Professional 4.2 and PowerBuilder Desktop and Enterprise versions 3.0/4.0. The tool has an interface that imports, exports, and updates PowerBuilder table structures and extended attributes. It costs $995. **Evergreen CASE Tools Inc**, Redmond, WA. (206) 881-5149. **Circle No. 399**

16-bit embedded controllers. The MQX16 real-time executive requires 3 kbytes or less of ROM. It is written in ANSI C, and can be extended by integrating real-time executive components from the company's standard MQX product. The executive provides functions such as task switching, pre-emptive scheduling, memory management, time stamping, delaying, and interrupt management. The product is available for the Motorola 68HC11 and Intel 8088 and 80x86 processors. A project-based, royalty-free, source-code license, including one PC-based executable, costs $3000. **Precise Software Technologies Inc**, Nepean, ON, Canada. (613) 596-2251, ext 27. **Circle No. 400**

Embedded DOS runs Windows. Embedded DOS 6-XL is compatible with Microsoft DOS 5.x and 6.x and provides real-time, fully pre-emptive, multitasking with 32-bit thread support. It comes with a set of 48 kernel services callable from C or assembly and includes threads, timers, events,

mutex semaphores, and memory pool. The operating system is available in binary and full-source adaptation kits for $995 and $2500, respectively. **General Software**, Bellevue, WA. (206) 454-5755. **Circle No. 401**

ICEs for Motorola's MCF 5102. The CodeICE system couples a full-featured in-circuit emulator (ICE) with a debugger. The MWX-ICE debugger operates on Sun 4, HP 9000, and Windows PC platforms. It supports popular compilers, including MRI and DIAB Data. The emulator is available with a run-control system, 4 Mbytes of overlay memory, a 32k-word trace system, and a multithreaded event system. Prices start at $21,950 for a PC-based system with 32k-word trace memory and no overlay memory. **Applied Microsystems Corp**, Redmond, WA. (206) 882-2000. **Circle No. 402**



Development tool simplifies the creation of imaging applications. The ImPowerTools let you create imaging applications for deployment on Novell LANs and Windows-based PCs without writing code. The tool kit also includes AppWare loadable modules for scanner, viewer, ICR, OCR, index, store, retrieve, and print functions. According to the company, the tools let you create customized imaging applications in hours or days, instead of weeks or months. Prices for the tools start at $7500 for a five-seat license. **Alta Technology Corp**, Sandy, UT. (801) 562-1010. **Circle No. 403**

FDDI, LAN, SCSI, and ATM cards use PCI mezzanine-card architecture. The new products using the Peripheral Component Interconnect (PCI) Mezzanine Card (PMC) architecture are: The MPMC221 fibre-distributed-data-interface (FDDI) adapter, the MPMC201 high-performance 100VG AnyLAN adapter, the MPMC101 high-end fast and wide SCSI-2 communications controller, and the MPMC281 asynchronous-transfer-mode (ATM) adapter. Prices for the cards start at $550. **Motorola Computer Group**, Tempe, AZ. (800) 624-6449. **Circle No. 404**

Programming environment for embedded systems has sophisticated editors for C and assembly. The Embedded Development Environment (EDE) is available for 8051, MCS 251, MCS 96, 68HC08, 80C166, and R3000 devices. The EDE shell provides a consistent interface to the tools for creating, editing, building, and debugging an embedded application. It includes a high-level C- and assembly-language editor, a C interface generator, a make tool, a librarian, object-code and cross-reference report writers, for-

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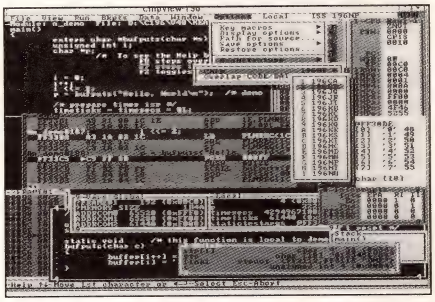
matters, and converters. You can extend the tool set to include other tools from the company and interfaces to other company's tools. EDE costs $229. **Boston Systems Office/Tasking**, Dedham, MA. (617) 320-9400.
Circle No. 405



High-level debugger for 80196 C compilers and assemblers. ChipView-196 version 1.0 is derived from the company's ChipView-51 products and is compatible with Borland's Turbo Debugger. The debugger supports all phases of design and test with a single user interface. The system includes an instruction-set simulator/debugger, a high-level user interface for CheckMate Systems' 80196 emulator, and a reduced-instruction-set monitor (RISM) based on a ROM monitor debugger. The system costs $795 for the instruction-set-simulator version and $995 for the RISM-based ROM-monitor version. **ChipTools Inc**, Mississauga, ON, Canada. (905) 274-6244.
Circle No. 406

Real-time modular development system for 16- and 32-bit microcontroller families. The MMDS1632 hardware- and software-development system provides real-time in-circuit emulation for the company's 68HC16 and 68300 microcontroller families. The modular system comprises a station module, a device-specific microcontroller personality board, package-specific personality and target boards, emulation software, and the necessary interfaces. The modular approach lets you configure the system for a range of applications at minimum cost, because you need to purchase only the modules necessary for your application. The MMDS1632 costs $12,500, and prices for microcontroller personality boards start at $500. **Motorola Microcontroller Technologies Group**, Austin, TX. (800) 765-7795, ext 912.
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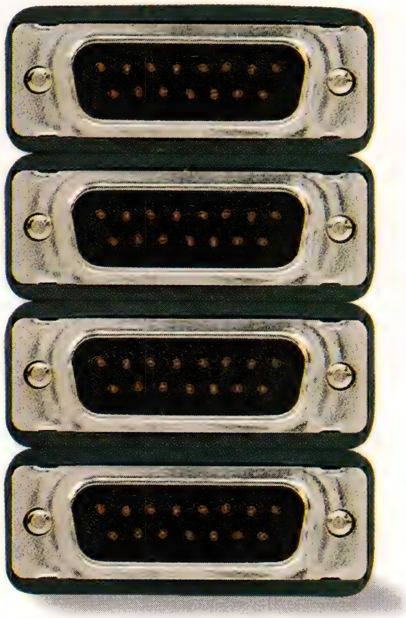

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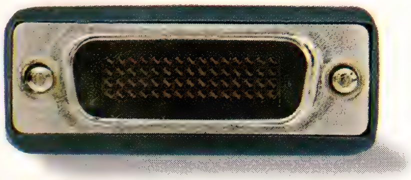

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RISC processor provides glueless interface to memory and other improvements. The MB86936 RISC processor is available in 30- and 60-MHz versions. It includes an 8-bit video interface to streamline rasterization and configurable bus sizing, so that the IC can accommodate 8-, 16-, and 32-bit memories. The processor also has a 4-kbyte instruction cache and a 2-kbyte, two-way set-associative data cache. Samples cost $80. **Fujitsu Microelectronics Inc**, San Jose, CA. (408) 922-9000. **Circle No. 363**

μC based on 8051 offers expanded feature set. The SABC509 8-bit μC has a 29-channel capture-compare unit, 3.3 kbytes of RAM, a 15-channel, 10-bit A/D converter with adjustable sampling and conversion times, a 60-kHz PWM unit, and up to 64 general I/O pins and 15 input-only pins. The device costs $12.60 (10,000). Other versions offering less RAM start at $2.37 (1000). **Siemens Components Inc, Integrated Circuits Division,** Cupertino, CA. (408) 777-4500. **Circle No. 364**

Communications processor for V.34 modem applications. The 68DP356 combines a general-purpose μP core, a RISC communications engine, and a 24-bit DSP. It provides the hardware and software to perform data-pump functions for V.34 modem applications. The processor works with the ST7544 codec from SGS Thomson Microelectronics to perform data-pump and controller functions. The processor costs $75.95 (10,000). **Motorola Microprocessor and Memory Technologies Group**, Austin, TX. (512) 891-2429. **Circle No. 365**

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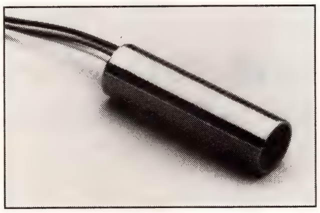
High-speed recording and real-time display package provides throughput rates to 400 kHz. This high-speed recording and real-time display package has throughput rates of 400 kHz to RAM disk and 330 kHz to a hard disk. The package provides triggered and continuous acquisition modes in 16-, 32-, or 64-channel configurations. From $4000. **RC Electronics Inc**, Santa Barbara, CA. (805) 685-7770. **Circle No. 367**

Portable SCSI performance and protocol analyzer attaches to PCMCIA socket. The SCSI-View Model SV-8020 measures 5.75×3.6×0.81 in. and attaches to a notebook PC via the PCMCIA socket. The instrument transfers captured SCSI phase-event information to the host computer for analysis with the software. The software can search captured files for phase times, incomplete commands, messages, status bytes, and data burst rates. The instrument includes reprogrammable field-programmable gate arrays, allowing the company to add analyzer features and other changes by software updates. The analyzer with software costs $2995. **Verisys Inc**, Soquel, CA. (408) 464-4292. **Circle No. 368**

Low-cost data-acquisition device connects to serial port. The 232SDA10 has 11 channels of 10-bit A/D conversion with a 0 to 5V input range, three digital inputs with a ±30V range, and three digital outputs with a 0 to 5V range. The module uses three commands and has automatic baud-rate detection from 1200 to 9600 baud. The 10-bit version costs $49.95, and a 12-bit version costs $59.95. RS-485-compatible modules are also available. **B&B Electronics Manufacturing Inc**, Ottawa, IL. (815) 434-0846. **Circle No. 369**



Hall-effect sensor works over wide range of air gaps. The Model 427008-30 zero-speed noncontact sensor senses targets at speeds from 0 to 20,000 Hz. It operates over air gaps ranging from 0.010 in. for 44-pitch gears to 0.120 in. for eight-pitch gears. The 0.375-in.-diameter×1.4-in.-long sensor is available in a standard model rated for 105°C and a high-temperature model rated for 150°C. Samples costs $75. **Magnetic Sensors Corp**, Anaheim, CA. (714) 630-8380. **Circle No. 370**

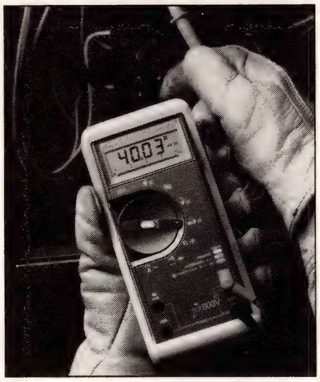
I/O board provides interface between commercial test equipment and custom designs. The Interface Control Board (ICB) provides embedded μP control of custom circuitry across an IEEE-488.2 or RS-232C interface. The board comes with 72 digital I/O lines, programmable timers, an interrupt timer, DMA circuitry, and several system clocks to control hardware. You can install custom circuitry in a prototype area and interface it to test circuitry through three 96-pin DIN connectors. The ICB is designed around a Eurocard 6U form factor and fits into a VME-type chassis, B-sized slot. The board, including RS-232C cable, daughterboard, and software, costs $995. **Advanced Designs Inc**, Colorado Springs, CO. (719) 598-9224. **Circle No. 371**

PCI bus analyzer performs 200-MHz timing and 66-MHz state analysis on all 96 PCI bus lines. The 64-bit PCI-BA+64 and the 32-bit PCI-BA+32 acquire and display timing or state information on all types of bus cycles for 64- and 32-bit PCI-based systems. The bus analyzers use the high-speed ECP parallel-port interface protocol to transfer data as fast as 2 Mbytes/sec to PCs running Windows. It stores as many as 256,000 samples for each of the 96 input lines. You can select the amount of pre-trigger and post-trigger information you want in the sample data. Eight external 200-MHz input channels are also available. The 64-bit board costs $6995, and the 32-bit board costs $4995. **NewBus Co**, Fremont, CA. (408) 929-9060. **Circle No. 372**

Instrument-driver DLL simplifies instrument control for Visual Basic and C users. The Instrument Driver dynamic-link library includes >75 instrument drivers for controlling popular IEEE-488 test instruments from Fluke, HP, Tektronix, Wavetek, and other instrument suppliers. The library is available on CD-ROM and costs $495. **National Instruments**, Austin, TX. (512) 794-0100. **Circle No. 373**

10-MHz direct digital-synthesis function generator costs $1269. The Model 29 function generator provides both standard and arbitrary waveform generation. Standard functions include sine, square, positive pulse, negative pulse, multi-level square, triangle, ramp-up, ramp-down, sin x/x, dc, and pseudorandom noise. The instrument includes both RS-232C and IEEE-488 interfaces for remote programming. Battery-backed memory stores nine instrument setups. **Wavetek Corp**, San Diego, CA. (619) 279-2200. **Circle No. 374**

Passive bus analyzer adds support for SCAM protocol. The IPC-6500 bus analyzer now supports SCSI Configured AutoMagically (SCAM), which Windows 95 requires on SCSI systems. The bus analyzer features a single-ended and differential line connector, 20-nsec resolution for 16- and 8-bit SCSI, event filtering using transition masks, a 50-MHz programmable state machine, 16-level triggering, and multiple data display modes. The hardware comes with a full-length ISA-bus card with 68- and 50- pin connectors. It costs $5100. **I-Tech Corp**, Edina, MN. (612) 941-5905. **Circle No. 375**



True-rms DMM meets IEC-1010 Category III standards. The Model 76 DMM for overvoltage Category III requirements continuously withstands 600V ac or dc and has impulse withstand protection up to 6000V. The DMM is either certified to or has pending certification to the following agency approvals: UL, CSA, CE, and

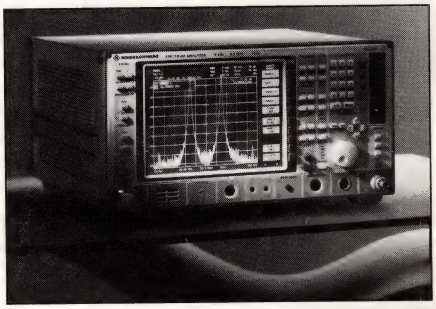
TUV. The 3½-digit, 4000-count multimeter measures true-rms ac voltage and current, dc voltage and current, resistance, frequency, capacitance, continuity, and diode test. It costs $199. **Fluke Corp**, Everett, WA. (206) 347-6100. **Circle No. 376**

16-bit data-acquisition boards for ISA bus have 10-μsec scanning per channel. The DaqBoard/200A provides 16 channels, expandable to 256 while maintaining the 10-μsec per channel scanning speed. The board also provides a 512-position sequencer for selecting the analog channel sequence and gain value in any order. The board has two 12-bit analog output channels supporting sample rates to 500k samples/sec, a high-speed 16-channel digital I/O port, a 24-bit general-purpose digital I/O port, and five independent 16-bit counter/timers. The board costs $1195. The DaqBoard/216A offers the same data-acquisition features without the digital I/O and counter/timers; it costs $995. **IOtech Inc**, Cleveland, OH. (216) 439-4091. **Circle No. 377**

Extenders for ISA bus provide hot-swap and other debug features. The PC/AT150 extender for 8-bit ISA bus and the PC/AT200 for 16-bit ISA bus cards let you add and remove cards without turning off the system power. The feature adds a 250-psec propagation delay and a 4Ω on-resistance, causing minimal degradation in performance for the board under test. The extenders also provide short-circuit protection and current limiting to avoid motherboard damage. The extender generates a power-on reset signal whenever the extender board is turned off and on. DIP switches let you selectively isolate signals for debugging. The PC/AT150 costs $295, and the PC/AT200 costs $345. **Catalyst Enterprises Inc**, San Jose, CA. (408) 268-4145. **Circle No. 378**

64-Mbyte oscilloscope-memory option accommodates waveform processing of long records. The 930X-64 option for the company's 9300 series digital oscilloscopes lets you perform integration, differentiation, FFT, square, square-root, log, and exponential functions and use six selectable digital filters on data records up to 8 Mbytes long. The option costs $3500 and can be retrofitted into previously delivered oscilloscopes. **LeCroy Corp**, Chestnut Ridge, NY. (914) 425-2000. **Circle No. 379**

Pen-style DMM has 4200-count display. The DM73A has a reading-hold feature to freeze a reading. It also automatically holds maximum voltage readings and minimum resistance readings. The meter has an automatic shut-off for extended battery life. It is designed to UL and EN (IEC) agency safety standards. $69.95. **Wavetek Corp**, San Diego, CA. (619) 279-2200. **Circle No. 380**

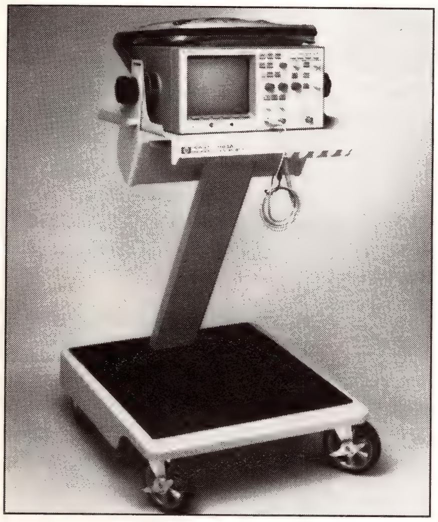


Fast spectrum analyzers cover frequencies from 20 Hz to 3.5 GHz. The FSEA 20 spectrum analyzer operates from 9 kHz to 3.5 GHz and costs $29,995. The FSEA 30 spectrum analyzer covers frequencies from 20 Hz to 3.5 GHz and costs $43,895. Specifications include a resolution bandwidth of 1 Hz to 10 MHz, an intermodulation-free dynamic range of 113 dB, a noise floor of –145 dB for a 10-Hz bandwidth, and a phase noise of –123 dBc/Hz at 10-kHz offset. The instruments evaluate the performance of mobile communications systems. Rohde & Schwarz developed the analyzers, which Tektronix market and support in the United States and Canada. **Tektronix Inc**, Beaverton, OR. (800) 426-2200. **Circle No. 381**

Tool creates boundary-scan-description-language files from Verilog netlists. BSDLMaker compiles structural Verilog netlists and package pin files, performs 1149.1 design-compliance checks, and generates a boundary-scan-description-language (BSDL) file. The tool also provides a warning- and error-message file and a debug file. You can configure the tool to accept primitives and macrocells from multiple silicon vendors, such as LSI Logic, TI, VLSI, and others. The software costs $6750 for PCs and

$8100 for the Sun SPARC. **Intellitech Corp**, Meredith, NH. (603) 279-6308.
Circle No. 382

PC software lets you document, archive, analyze, and create waveforms for test instruments. AnyWave 2.0 is for the company's ScopeMeter, CombiScope oscilloscopes, and ARB generators. The software lets you create waveforms from scratch using a mouse or modify waveforms captured by an oscilloscope. You can use the waveforms in the PM 5150 arbitrary waveform generator or on the oscilloscopes for pass/fail testing. The software communicates to the instruments through RS-232C or IEEE-488 interfaces and costs $295. **Fluke Corp**, Everett, WA. (206) 347-6100.
Circle No. 383



Cart holds logic analyzers and oscilloscopes. The HP 1183 Testmobile holds the HP 54620A logic analyzer and the HP 54600 oscilloscopes. A locking system attaches the instrument to the cart. You can lock the tray holding the instrument into various positions. The tray also has a holder for scope probes. The cart costs $495. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844, ext 9422. **Circle No. 384**

Computer-aided-experiment design package for Windows. The Computer Aided Research and Development (CARD) software suits use by scientists and engineers working in product, process, and quality R&D. The tool helps you design experiments to get the information you need from the experiment. It handles multilevel experiments with mixture variables and multiple constraints. The software costs $495. **Westing Software**, Corte Madera, CA. (415) 945-3870.
Circle No. 385

Compact power meter has wide power level and frequency coverage. The Model 4220 power meter covers frequencies from 100 kHz to 100 GHz and measures power from –70 to +44 dBm. Dynamic range is up to 90 dB with diode sensors and 50 dB with thermocouple sensors. The meter fits into a half-rack panel, making it suitable for production automatic-test-equipment environments. It costs $2150. **Boonton Electronics Corp**, Parsippany, NJ. (201) 386-9696. **Circle No. 386**

Bus analyzer for IDE/ATA packet interface. The ID-520 IDE/ATAPI bus analyzer has 32 ATbus-attachment (ATA) channels plus four general-purpose channels. It has a 50-MHz sampling frequency, a 1-million-event capture buffer, and the ability to capture continuously to disk. The board and Windows-based software cost $6500. **Innotec Design Inc**, Buena Park, CA. (714) 522-1469. **Circle No. 387**

Low-cost programmer for Xilinx EPLD devices. The XPGM programmer for erasable PLD (EPLDs) and serial configuration PROMs (SPROMs) costs $295. Xilinx certifies the programmer to meet the programming criteria for all of the current EPLD and SPROM product lines. The programmer is an ISA bus card that connects with an external programming socket via a 30-in. ribbon cable. It comes with adapters for 44-pin PLCC packages and eight-pin DIP packages. Adapters for other packages cost $99 to $199. **Deus Ex Machina Engineering**, St Paul, MN. (612) 645-8088. **Circle No. 388**

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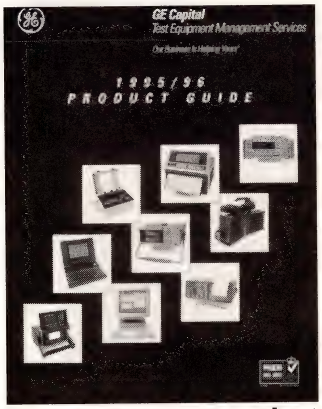
Catalog for system-power products. A catalog features technical information on a range of products, including alternate current sources, dc power supplies, and electronic loads. The 66-pg guide contains application information, dimension drawings, photos, and product specifications. **Hewlett-Packard Co**, Santa Clara, CA. **Circle No. 350**

Brochure presents power supplies for displays. A guide for a line of information-display power supplies includes dc/ac inverters for cold-cathode-fluorescent-tube, backlit LCDs. The brochure features a line of dc/dc converters for applications such as gas-plasma displays. **Endicott Research Group**, Endicott, NY. **Circle No. 351**

Interactive catalog on disk. This interactive computer program guides users through the selection and configuration of a line of power supplies, including modular components and configurable systems. The catalog includes power-system accessories. **Vicor Corp**, Andover, MA. **Circle No. 352**

Hypertext Markup Language pocket reference. A reference card details the Hypertext Markup Language, the language of the World Wide Web. The fold-out card shows how to format a Hypertext document for use with the World Wide Web, including how to lay out text and how to set up headers, titles, and tables. The guide also describes the types of forms, how to set up a point-and-click mat, and how to include anchors, sounds, and images. $4.50. **Specialized Systems Consultants Inc**, Seattle, WA. **Circle No. 353**



Test-equipment product guide. This catalog features rental equipment for testing power-transmission and distribution, communications, industrial-plant operations, and microwave/RF systems. The guide describes the company's one-source repair, calibration, and certification services. **GE Capital Test Equipment Management Services**, Norcross, GA. **Circle No. 354**

Trimmer-capacitor catalog. This 34-pg catalog describes a line of glass, quartz, air, and trimmer capacitors. The guide details sample kits, tuning tools, and design capabilities. **Voltronics**, Denville, NJ. **Circle No. 355**

Catalog features components. A detailed catalog offers specifications for a product line, including triacs, SCRs, rectifiers, and diacs. The guide provides diagrams, application notes, and a cross-reference guide. **Teccor Electronics Inc**, Irving, TX. **Circle No. 356**

Handbook covers Windows software. This guide highlights software under DT-Open Layers for Microsoft Windows 95 Plug-and-Play. It covers numerous programming tools, a new high-level DSP language and compiler, and visual-programming applications. **Data Translation**, Marlborough, MA. **Circle No. 357**

Satellite-wire-and-cable guide. This free guide highlights lightweight wire and cable for commercial, military, and NASA satellites. The brochure details a radiation-cross-linked insulation system. **Raychem**, Menlo Park, CA. **Circle No. 358**

Catalog details sensors. This catalog provides diagrams, dimensions, and specifications for a line of photoelectric sensors. The guide includes a detailed accessories guide. **Aromat Corp**, New Providence, NJ. **Circle No. 359**

Guide for Teflon pc-board prototypes. *What Does it Take to Get a Good Teflon Circuit Board Prototype Around Here?* is a guide to fabricating Teflon prototypes. The guide details a Teflon prototyping service for microwave and wireless-applied pc boards. **Southwest Circuits**, Tucson, AZ. **Circle No. 360**

Power-switches and regulators data book. This catalog contains data sheets on more than 50 devices, including single- and dual-output linear regulators, switching regulators, and power-supply-control ICs. The guide features an expanded section of application notes on topics such as hysteretic mode control. **Cherry Semiconductor**, East Greenwich, RI. **Circle No. 361**

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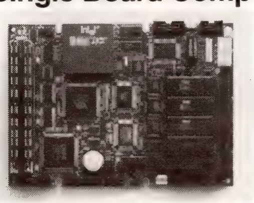

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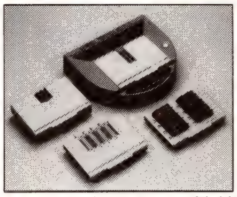

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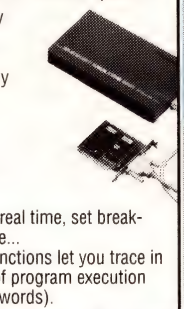

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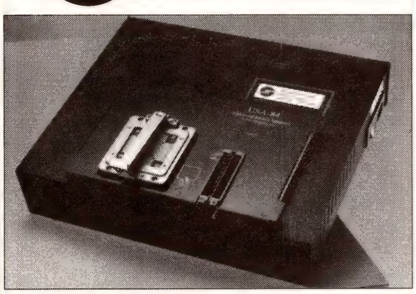

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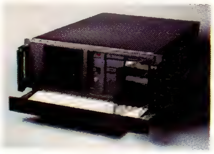

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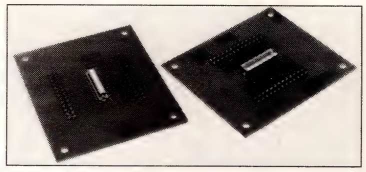

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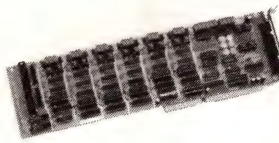

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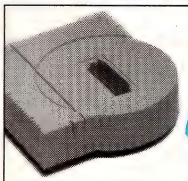

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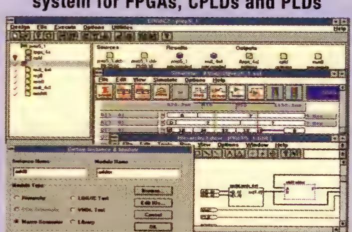

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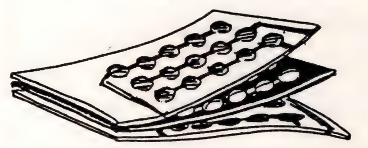

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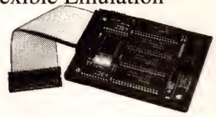

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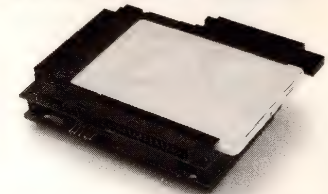

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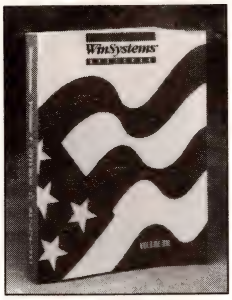

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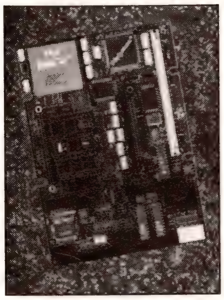

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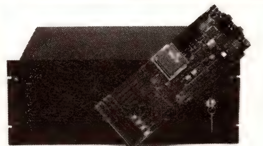

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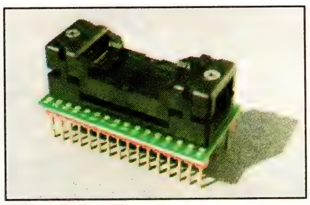

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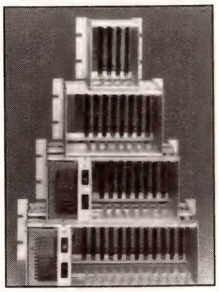

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Company	Page	Circle
3M	156	264
Accutrace Inc	155	250
Advin Systems	155	253
American Advantech Corp	155	251
Analog Devices Inc	21	205
Analogic Corp	133	212
Ancot Corp	154	49
Applied Micro Circuits Corp	43	137
Archimedes Software Inc	144	33
Arnold Magnetics Corp	143	32
Audio Precision	169	136
Bourns Inc	45	138
Burr Brown	103	139
Bytek Instruments System	158	275
Caig Laboratories Inc	152	47
Calyx Systems	156	263
Capilano Computer Systems Inc	159	280
CEIBO	158	278
Condor D.C. Power Supplies	59	144
Crystal Semiconductor	57*	145
Cypress Semiconductor	C4	
Dallas Semiconductor	17	146
Data I/O Corp	156	260
Data Translation Inc	57	147
Datel Inc	67	148
Digi-Key Corp	1	1
	79	149
Ecliptek Corp	129	26
EDI Corp	159	286
Elantec	170	153
Electronic Engineering Tools	156	257
Elgar Corp	148	154
Embedded Support Tools Corp	130	27
Ericsson Components AB	122	155
Eurom Flash Ware Solutions	67*	228
Fujitsu Ltd	80-81	125
Gilway Technical Lamp	130	28
Gould Electronics Inc	157	266
Hamilton Hallmark	23	
Harris Semiconductor	60A-N	
Hewlett Packard	6-7	
Hirose Electric USA	156	258
Hitachi America Ltd	94A-H	
IEE	98	121-122

Company	Page	Circle
Innovative Software	157	267
Integrated Device Technology	121	
Intel Corp	46-49	
International Rectifier	C3	156
Interpoint	117	157
Intusoft	115	158
Ironwood Electronics	157	265
IS Data GmbH	156	262
Janco Corp	132	29
Keil Software Inc	134	159
LeCroy Corp	14	160
Linear Technology	77-78	
	135-138	102-113
Link Instruments	157	269
Littelfuse Inc	91	161
Logical Devices Inc	157	268
M-Systems	145	36
Maxim Integrated Products	71	92-93
	73	94-95
	75	96-97
MCSI	156	259
Metalink Corp	159	288
MicroSim Corp	19	162
Minc Inc	159	282
Mini Circuits	3	185
	39	186
	41	187
	69	188
Mitsubishi Electronics America	93	163
	94	164
Molex	147	189
Motorola Inc	111-113	
Motorola Semiconductor	62-63	
Murata Electronics	125-127	203
National Instruments	61	3
	153	48
National Semiconductor	9-13	
NEC Corp	96-97	211
Nichicon	158	279
Nohau Corp	84	213
OrCAD	C2	214
Pacific Softworks	146	37
Philips Semiconductor	104-105	
Pico Electronics	128	215
	139	30
	168	30
Prima International	146	38
Printed Circuit Technology	144	34
Programmable Designs	158	277
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Company	Page	Circle
Quicklogic	60	218
Raltron Electronics	74	9
Samsung Display Devices	14*	10
Samsung Semiconductor	82-83	210
Semtech Corp	131	11
Siemens AG	50-51	165
Sierra Circuits	155	255
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Stanford Research	151	13
Synopsys	106	
Tatum Labs Inc	157	270
Tech Tools	158	272
Teledyne Relays	76	17
Tern	158	273
Texas Instruments	28-31	91
	89	12
	100-101	19
Thermo-O-Disc Inc	74	4
Tokin Corp	118	66
Toshiba America Electronic Components	26-27	
	142	
Toshiba Europe	26*	
	27*	
Tribal Microsystems	155	252
US Logic	159	285
Unitrode Integrated Circuits	52	8
	8	
VME Microsystems Intl Corp	141	123
Volgen America	149	39
WL Gore	149	46
Wavetek Corp	140	31
WinSystems	159	287
Z-World Engineering	157	271
Zaxtek	158	274
Zendex Corp	156	256
Ziatech Corp	164	2

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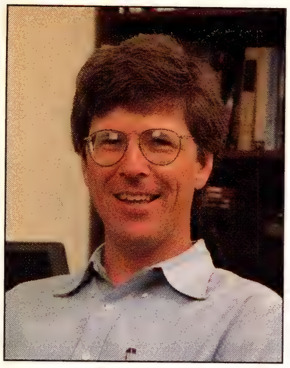

JACK GANSSLE, EMBEDDED-SYSTEMS CONTRIBUTING EDITOR

Living to learn

Colleges do a lousy job of preparing engineers for the real world. It's appalling that so little of typical curricula is dedicated to making things work; to experiencing dramatic failure in all its guises; or to taking an idea from inception, through design and debug, to functioning product.

Engineering is about making things. Although we need the theoretical grounding with which colleges seem so enamored, what differentiates us engineers from scientists is our focus on producing products. Things that work. Things that improve life for the masses. I love to make things, and I take great delight in the process of invention that leads to something that finally works.

It seems, however, that most young engineering graduates are convinced that their education is over. After four or five years of struggling through differential equations and organic chemistry, they think that studying is yet another of life's unpleasant obstacles they've finally overcome.

Balderdash.

Embedded design is a dynamic field that changes daily. The knowledge half-life is approximately two years; so, if you're not studying constantly, count on being obsolete before turning 30. Yes, it is possible to find a comfortable niche where you can park for a number of years—ignoring the advance of technology. But, when it's time to hit the job market, you may be shocked to find that everyone is speaking an incomprehensible language.

Although night courses are a great way to catch up with new programming methods like C++, it's tough to find universities offering state-of-the-art information about hardware design. Generally, the best courses are those that vendors offer. Any successful vendor is pushing the very latest technology, and many recognize that they must offer some sort of training. Take advantage of these opportunities—they're often free. Convince your boss that a day or two of training is time well spent.

Probably the best way to stay current is to read constantly and widely. Greedily suck ideas from *EDN* and other publications. Don't expect to understand everything immediately, and never give up the battle just because you don't understand the concepts. The larger goal is to learn new ideas!

> ***Spend time in good bookstores. Never has so much information been available in so many easily digestible forms.***

Blow up your TV

Spend time in good bookstores, both the "real" and the virtual order-by-mail varieties. Never has so much information been available in so many easily digestible forms. Although lots of books still resemble those heavy tomes we slogged through in college, many now are fun and almost lighthearted—even when equations litter the pages.

Every embedded-hardware designer should read *High Speed Digital Design (a Handbook of Black Magic)* by Howard Johnson and Martin Graham (PTR, Prentice Hall, NJ, 1993). Although the book may be challenging if your grasp of theory is rusty, it's worth reading even if you have to skip the math.

Modern components are so fast that even slowly clocked systems suffer from all sorts of speed problems. This book leaves little unanswered in the quest for reliable digital designs.

PHOTOGRAPHY / HOWARD DAVIS

The authors cover transmission-line theory in detail. At first glance, I shuddered, remembering two incomprehensible semesters of electromagnetics. Johnson and Graham balance theory with lots of practical information. For example, a right-angle bend on a pc-board trace is a transmission disaster, which you can cure simply by rounding the track edges.

Most engineers are vaguely aware that corrupting a pc-board ground or power plane is not a good move. Sometimes, though, the temptation to save a couple of layers by routing a couple of tracks on the power plane is overwhelming. In just a few paragraphs, this book shows why this is a horrible idea, as the current return for any track runs under the track itself. Even designers with the best of intentions may accidentally create this situation by poorly specing hole sizes for connectors. If the holes are too large, they may intersect, creating a similar, though unintended, slot.

The book also includes an entire chapter explaining the best way to stack layers on a pc board. One criticism, however, is that I would like to see more discussion on how signals couple with different stack configurations.

Vias, too, get their own chapter. There's lots of good advice. The best sound bite is that small vias are much faster than larger ones. Small vias surely help routing, too, especially with SMT boards, so there's a ray of hope for us yet!

One of the biggest challenges digital designers face is propagating signals off-board through cables. A single chapter on this subject is worth the entire price of the book. Ribbon cable is far better than I realized, especially when you run grounds, as the authors recommend.

What's the best way to use a scope on a high-speed system? What is the effect of that short ground wire coming from the probe? It turns out that the 3-in. ground lead can degrade the displayed rise time by more than 4 nsec! The authors offer the best description of scope-probe problems (and solutions) I've ever seen. They show how to build a better probe using parts found in any shop.

One of the biggest challenges digital designers face is propagating signals off-board through cables.

Did you know that skin effect, the tendency of high-frequency signals to travel only in the outer edges of a conductor, can become important on pc-board tracks at frequencies as low as 4 MHz? Halving the length of a conductor improves its frequency response by a factor of 4. Until reading this book, I was under the impression that only RF designers needed to worry about this effect.

Read this book. Then pass it along to your pc-board designers.

Bebopping along

Clive Maxfield's book *Bebop to the Boolean Boogie* (Hightext Publications, Solana Beach, CA, 1995) is the MTV version of an embedded-design how-to book. It's fun. It's a fast read. You'll find neither calculus nor much about basic electronics. It focuses entirely on logic design. The book is designed as a primer for those without much grounding in this area. (For a full book review, see *EDN*, Out In Front, April 27, 1995, pg 28.)

Hardware designers who've been at this for a couple of years probably have mastered the material already. It appears, however, that the embedded world is evolving into two camps—digital design and firmware—with less and less communication between the two. Increasing specialization means there are fewer people who can deal with systemwide problems. If you are an embedded-software guru who just doesn't understand the electronics part of the profession, get this book and spend a few delightful hours getting a good grounding in digital-design basics. Then watch for startled looks as your water-cooler discussions include comments about state-machine design.

Bebop covers all the basics, from the history of number systems (much more interesting than the tiresome number-system discussions found in all elementary texts), to basic logic design, PALs, and even pc-board issues. I often meet engineers who have no idea how chips are made; this book gives a great, easily readable, overview of the process.

Its discussion of memories is fast-paced and worthwhile. A chapter about DRAM RAS/CAS operation would be a nice addition, as would some material on flash, but there's a limit to what you can pack into 450 pages.

I found the chapter about linear feedback shift registers the most interesting. This subject never fades away. It pops up constantly on the embedded-systems Internet list servers (comp.realtime and comp.arch.embedded), often under the guise of CRCs. These pages are worthwhile reading even for experienced digital engineers.

And, yes, the seafood-gumbo recipe in Appendix H is worth the entire price of the book.

Jan Axelson's *The Microcontroller Idea Book* (Lakeview Research, Madison, WI, 1994) is an ideal introduction to low-end embedded design. The book's focus is the 8052-Basic CPU, a very-low-end controller suited for designers with no assembly-language or C expertise. Axelson takes the reader from essentially no knowledge of programming through Basic while offering lots of insight into the design of simple embedded systems. This work is much too simple for the experienced engineer but is worthwhile for the novice embedded designer.

The next time I hire new CS or EE graduates, I plan to have them work through both *Bebop* and *The Microcontroller Idea Book*. A week spent soaking up these practical concepts will help ground them in reality and balance the four years of theory still ringing in their ears.

Another Hightext Publications book, *Programming Microcontrollers in C* by Ted Van Sickle (Solana Beach, CA,

1994), is a succinct introduction to embedded firmware. Whereas *Bebop* is ideal for the digital-designer wannabe, *Programming Microcontrollers in C* is a must-read for engineers trying to get a handle on software issues.

In 88 pages, Van Sickle gives a complete and easily readable introduction to C programming. The book offers advice alongside programming facts. Here's an example: "Programming is a contact sport, so don't expect to become a C whiz till you've written and debugged a few thousand lines of code." The book's discussion offers a great starting point for designers seeking to broaden their background in C.

If you're using the 68HC11 or 68HC16, I'd advise looking through the book to get a feel for what these CPUs can do. The text is definitely not an advanced user's guide, but it gives a nice overview of using timers, pulse-width modulators, interrupts, and the like. Be forewarned, however, that the book doesn't provide much information on other chips.

> ***Frustration is a part of learning, so practice patience.***

Even better is its discussion about using Byte-Craft and Intermetrics compilers. Everyone dreads setting up a new environment. This book eases the process, especially since it includes header files.

I get a constant stream of queries for introductory texts to the embedded-systems world. This is the book. It should be required reading even in computer curriculum, where embedded systems get virtually no mention.

Plan for your future

Space limits the number of books I can cover here—and permits only the most cursory of reviews. More important than a discussion of any one book, however, is developing a philosophy that embraces continuous learning. As a parent, one of my greatest goals is to instill a love of learning and to ensure competence in reading for my children. All else follows from this; without it, nothing but intellectual stagnation is possible. In addition, consider the following:

- Never succumb to the temptation to let someone else dictate your career. Too many professionals avoid training because their company won't pay for it. That's career suicide. Take charge of your future, *yourself*, because no one else will.
- Frustration is a part of learning, so practice patience. Most engineering texts border on the unreadable. Cull the best of the bunch, and don't become frustrated when yet another book disappoints. Continue to seek out the pearls.
- Avoid excessive specialization. My dad relates the story of an engineer at Grumman in the early 1960s who knew everything there was to know about designing wheels for lunar-roving vehicles. Presumably pencil-cup donations are keeping the family fed now.

And, finally, take time to read a little poetry, some science fiction, and literature. The greatest ideas often originate from engineers who exercise their mental muscles in many diverse areas.

Jack Ganssle is the president of Softaid, a vendor of emulators and other embedded-systems tools. He can be contacted via Compuserve at "76366,3333," or via Internet at "jack@softaid.com." For those users of the Pony Express send mail c/o Softaid, 8310 Guilford Rd, Columbia, MD 21046.

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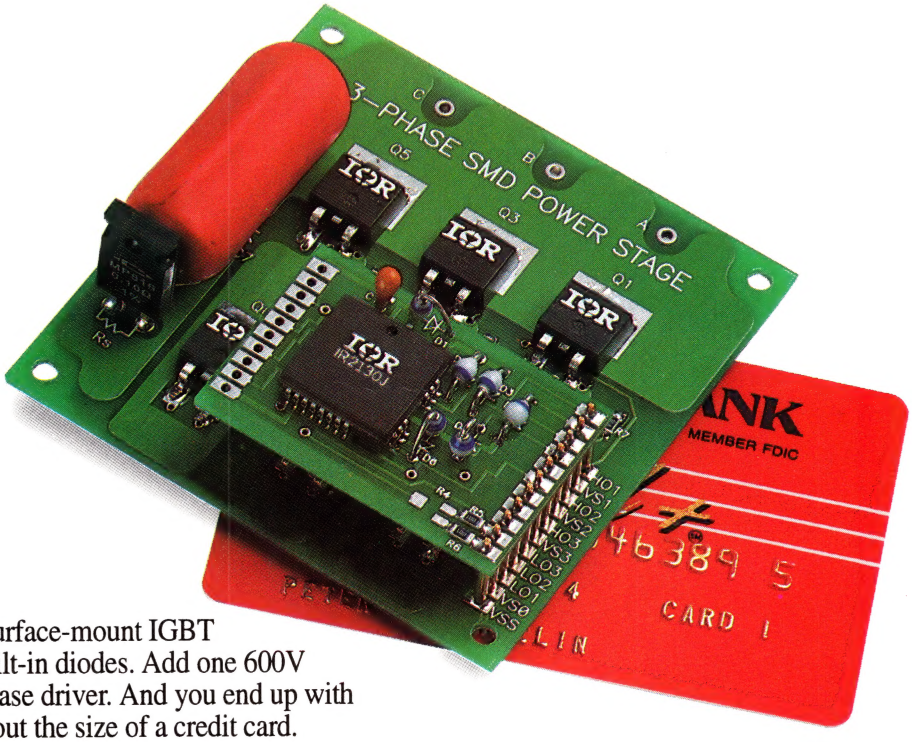

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